KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 405 Design and Modeling of Digital Systems
Term 062 Lecture Breakdown

Lec#	Date	Topics	Ref.
1	S 17/2	Syllabus, Introduction, Digital system design cycle, Architecture design.	Ch. 1
2	M 19/2	Architecture Design Example: 8-bitadder, Alternative adder designs including RCA, CLA, Serial Adder, Design Space.	Ch. 1
3	W 21/2	Behavioral Synthesis: scheduling and allocation, Digital system complexity, Hierarchy, Abstraction, Design domains and levels of abstractions, Design method, Synthesis vs. Design, Synthesis process.	Ch. 1
4	S 24/2	Circuit Synthesis, Design Automation & CAD tools, Hardware description languages, Objectives & requirements of VHDL, Styles in VHDL, Design flow in VHDL, Simulation Process. VHDL Basics: VHDL terms, Design entity. Entity Examples.	Ch. 1 & Ch. 2
5	M 26/2	Design Architecture, Architecture Examples: Full Adder, Ones count circuit.	Ch. 2
6	W 28/2	Alternative architectures for one's count circuit: behavioral, dataflow, structural. Elements of VHDL: Entity, Architecture, Package, Library, Configuration.	Ch. 2
7	S 3/3	Top down design methodology, Recursive partitioning, Design verification, Top down design of serial adder: 2x1 MUX, D-FF, 3-bit Counter, Behavioral model of serial adder.	Ch.3
8	M 5/3	Serial Adder First Level of Partitioning, Shifter VHDL Description, Structural Description of Serial Adder , Partitioning Shifter, Synthesizable Serial Adder, Subprograms: Procedure & Function Examples, Controller Description: Sequence Detector Example.	Ch.3
9	W 27/3	VHDL Predefined Operators, VHDL Lexical Elements: VHDL Design File, Delimiters & Identifiers, User Defined Identifiers, Literals: Character Literal,	Ch.3 & Handout

		String Literal, Bit String Literal, Abstract (Numeric) Literals, VHDL Language Grammar. VHDL Objects.	
10	S 10/3	Variables vs. Signals, Signal Assignment, Signal Transaction & Event, Delta Delay.	Ch. 4
11	M 12/3	Transport and Inertial Delay, Sequential Placement of Transactions.	Ch. 4
12	W 14/3	Sequential Placement of Transactions, Signal Attributes. Structural Specification of Hardware, A Cascadable Single-Bit Comparator .	Ch. 4 & Ch. 5
13	S 17/3	Structural model of a single-bit comparator, use of configuration statement. **(Quiz#1)**	Ch. 5
14	M 19/3	Netlist Description of Single-Bit Comparator, 4-Bit Comparator Structural Iterative Wiring , "For ……. Generate" Statement, "IF …… Generate" Statement Structural Test Bench.	Ch. 5
15	W 21/3	Ripple Carry Adder Design using Generate Statement. Synthesis using Xilinx. Different Binding Schemes : SR Latch.	Ch. 5
16	S 24/3	Port Map Association, Default Binding, Use of Configuration Specifications, Sequential Comparator, Subprograms, Functions, Examples of Functions.	Ch. 5 & 6
17	M 26/3	**Quiz#2.**	
18	W 28/3	Procedure Specification, Procedure Usage, Examples of Procedures, Using Procedures in a Test Bench, Executing a Procedure.	Ch. 6
	Th 29/3	**MAJOR EXAM I**	
19	S 31/3	Packages, Package Declaration, Package Body, Package Examples. Design Libraries. **(Solution of Major Exam I)**.	Ch. 6
20	M 2/4	Standard and TEXTIO Packages. Examples using TEXTIO package.	Ch. 6
21	W 4/4	Package IEEE.Std_Logic_1164.	Ch. 6
22	S 7/4	Design Parameterization, Values Passed to Generic Parameters, Configuration Declarations.	Ch. 6
23	M 9/4	Configuration Nesting , Configurations and Generics: Configuration of the N-bit Register, Selective Configuration Of Generate-Statement Instances: 8-bit Parity Checker. Data Types, Scalar Data Types, Number Formats, Enumeration Data Type.	Ch. 6 & Ch. 7
24	W 11/4	Physical Data Type, Composite Data Types: Arrays, Unconstrained Arrays,	Ch. 7

		Unconstrained Comparator Unconstrained Comparator Test Bench Referencing Arrays & Array Elements.	
25	M 16/4	Referencing Arrays & Array Elements, Using Enumeration Types for Indexing,, Records, Aliasing, Subtypes	Ch. 7
26	W 18/4	Type Compatibility & Conversion, Closely Related Types , Mixed Type Arithmetic, Custom Type Conversion, Type Attributes, Array Attributes, Signal Attributes	Ch. 7
27	S 21/4	Project Discussion. **(Quiz#3)**	
28	M 23/4	Toggle FF Example, File Type & External File I/O, Overloading, DATA FLOW MODEL, Conditional Signal Assignment, Selected Signal Assignment, Signal, Assignment Examples, Multiplexing, 3-to-8 Decoder.	Ch. 7 & 8
29	W 25/4	Clocking, Block Statement, dataflow architectures, for Positive-Edge-Triggered DFF, Nested Block Statements, Data Flow Example.	Ch. 8
30	S 28/4	Multi-Driver Signals: Signal Resolution Function, Resolution Function Examples: ANDING, ORING	Ch. 8
31	M 30/4	Resolution of Guarded and Non-Guarded Signals, Signal Kinds: BUS & Register, Examples: Different Implementations of PTL Multiplexer, Disconnection Delay.	Ch. 8
32	W 2/5	Mealy machine example using Block Statements, Sequence detector example, General Mealy State Machine .	Ch. 8
33	S 5/5	Multiplier Design: Controller Model, Data Path Model, +ive Edge-Triggered Shift Register with Parallel Load. Behavioral Descriptions in VHDL: Concurrent Versus Sequential Statements.	Ch. 8 & 9
34	M7/5	Process Statement, Process Examples, Wait Statement, Conditional Control – IF Statement, Case Statement. Loop Control , FOR Loop, WHILE Loop, Next & Null Statements, A Moore 1011 Detector using Wait, A Moore 1011 Detector without Wait, Generalized VHDL Mealy Model, Generalized VHDL Moore Model, FSM Example.	Ch. 9
35	W 9/5	NO CLASS.	
36	S 12/5	Using Wait for Two-Phase Clocking, Assert Statement, Checking for Setup & Hold	Ch. 9

		Time, Handshaking.	
37	M14/5	Formatted I/O, VHDL Coding Styles for Synthesis, General Overview of Synthesis, VHDL Synthesis Subset, Constant Definition, Port Map Statement, When, Statement, With Statement, Case Statement, For Statement, Generate Statement, If, Statement, Variable Definition.	Ch. 9 & Handout
	T 15/5	**MAJOR EXAM II**	
38	W 16/5	Multiplexor Synthesis, 2x1 Multiplexor using Booleans, 2x1 Multiplexor using a Process, Decoder Synthesis, 3-to-8 Decoder , Architecture of Generic Decoder, A Common Error in Process Statements, Another Incorrect Latch Insertion , Avoiding Incorrect Latch Insertion, Eight-Level Priority Encoder.	Appendix B & Handout
39	S 19/5	Ripple Carry Adder, Tri-State Buffer Synthesis, Bi-directional Buffer Synthesis, Latch Synthesis, Flip-Flop Synthesis with Asynchronous Reset, Flip-Flop Synthesis with Synchronous Reset, 8-bit Loadable Register with Asynchronous Clear, 4-bit Shift Register, Register with Tri-State Output, Finite State Machine Synthesis, Synthesis Static Sensitivity Rule, Impact of Coding Style on Synthesis Execution Time, Synthesis Efficiency Via Vector Operations, Three-State Synthesis.	Appendix B & Handout
40	M21/5	Latch Inference & Synthesis Rules , Flip-Flop Inference & Synthesis Rules, Alternative Coding Styles for Synchronous FSMs. CPU Design & Modeling Example.	Appendix B & Chapter 10 & Handout
41	W 23/5	**MAJOR EXAM II Solution.**	
42	S 26/5	CPU Design & Modeling Example.	Chapter 10
43	M28/5	Register Transfer Level CPU Modeling: Datapath & Control Unit Modeling.	Chapter 10
44	W 30/5	Review.	
45	S2/6	**Project Demonstrations.**	