COE 405, Term 162

Design & Modeling of Digital Systems

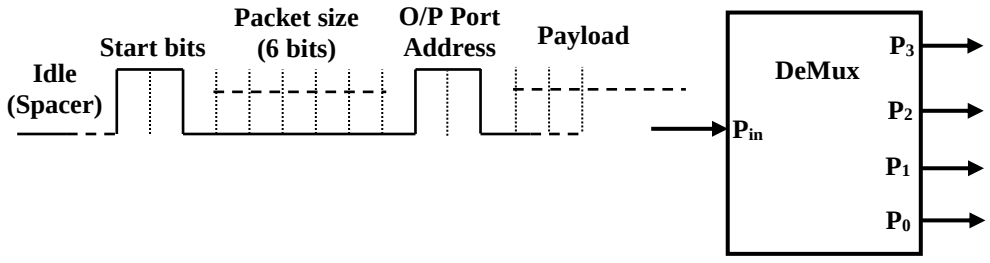
Assignment# 3

Due date: Sunday, April 9

It is required to design a simple network DeMux. The circuit has one input and four outputs (as illustrated in the figure below). Data packets arrive serially on the input and are routed to one of the four outputs:

- Packets have 10-bits headers,
- When the input line is idle (i.e. no data is arriving), it is kept low,
- A packet has two start bits (11), followed by 6-bits specifying the packet size in bits (i.e. from 0 to 63 bits), followed by two bits specifying the address of the output port (0 to 3), and immediately followed by the payload (i.e., packet data),
- The DeMux strips out the header before outputting the packet's payload,
- Whenever data is not transmitted across any of the output ports, its output line will be 0,
- Assume that packet size, port address and data will be transmitted from least significant to most significant bits,
- The circuit should be fully synchronous with an external clock and have a master asynchronous reset input.

The diagram below shows the block diagram of the circuit and the data format.



(i) Determine the required data path blocks to design this circuit along with their control signals (show the block diagram of these circuits only).

(ii) Show the block diagram of the data path and control unit and all the interface signals.

(iii) Obtain the ASMD chart of the control unit that will control the operation of the circuit.

(iv) Design the control unit using D-FFs and any other components of your choice.

(v) Model the data path in Verilog.

(vi) Model the control unit in Verilog based on your derived implementation in (iv).

(vii) Write a Verilog test bench to test the correct functionality of your implementation of the circuit. You test bench should send two packets one of size 4 bits addressed to port 0 transmitting the Hex. Value B and the second packet is of size 8 bits sent to port 2 transmitting the decimal value 9A.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a PDF file that contains the following items:

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.