COE 405, Term 162

Design & Modeling of Digital Systems

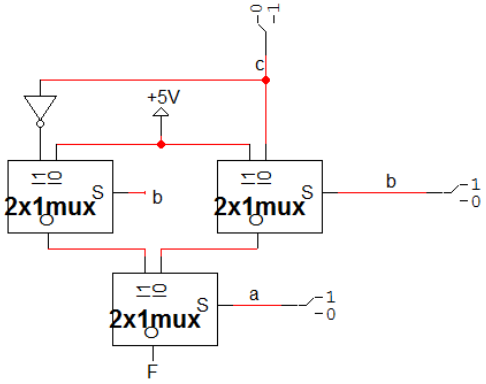
Assignment# 1 Solution

Due date: Saturday, March 4

Q.1. Consider the two functions f=(a ⊕ b) + (a ⊕ c) and g=a b + a' c + b' c'.

(i) Implement the function f using only 2x1 MUXs and inverters minimizing the number of MUXs used.

f = a' (b + c) + a (b' + c')
  = a' (b' (c) + b (1)) + a (b' (1) + b (c'))



(ii) Compute the function f⊕g based on orthonormal basis expansion.

f = a' b' (c) + a' b (1) + a b' (1) + a b (c')

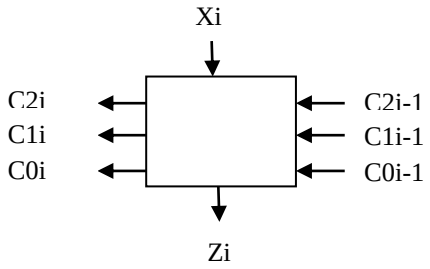
g = a' (b' + c') + a (b + c')
  = a' (b' (1) + b (c)) + a (b' (c') + b (1))
  = a' b' (1) + a' b (c) + a b' (c') + a b (1)

f⊕g = a' b' (c⊕1) + a' b (1⊕c) + a b' (1⊕c') + a b (c'⊕1)
  = a' b' (c') + a' b (c') + a b' (c) + a b (c)
  = a' c' + a c

Q.2. It is required to design an iterative combinational circuit that computes the equation Z=3*X-3, where X is an n-bit unsigned number.

(i) Determine the number of inputs and outputs needed for your 1-bit cell. Explain the meaning of values in the interface signals.

This circuit can be designed by assuming that we have a borrow of 3 feeding the first cell or by representing -3 as -1+-1+-1 where -1 is represented in 2's complement as 11…111 and thus adding 3 to each cell. I will follow the second approach. We need to represent carry-out values in the range 0 to 5. Thus, we need three signals to represent Carry out values propagation across cells.



(ii) Derive the truth table of your 1-bit cell.

$C1_{i-2}$	$C1_{i-1}$	$C0_{i-1}$	X_i	$C2_i$	$C1_i$	$C0_i$	Z_i
0	0	0	0	0	0	1	1
0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	1
0	1	0	0	0	1	0	1
0	1	0	1	1	0	0	0
0	1	1	0	0	1	1	0
0	1	1	1	1	0	0	1
1	0	0	0	0	1	1	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	0	0
1	0	1	1	1	0	1	1
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

(iii) Derive minimized equations for your 1-bit using K-Map method.

	00	01	11	10
00	1 0	0 1	1 3	0 2
01	1 4	0 5	1 7	0 6
11	?12	?13	?15	?14
10	1 8	0 9	111	010

Zi = C0i-1' Xi' + C0i-1 Xi = (C0i-1 ⊕ Xi)'

	00	01	11	10
00	1 0	1 1	1 3	0 2
01	0 4	0 5	0 7	1 6
11	?12	?13	?15	?14
10	1 8	1 9	111	010

C0i = C1i-1' C0i-1' + C1i-1' Xi + C1i-1 C0i-1 Xi'
= C1i-1' (C0i-1' + Xi) + C1i-1 C0i-1 Xi'
= C1i-1 ⊕ (C0i-1' + Xi)

	00	01	11	10
00	0 0	1 1	1 3	1 2
01	1 4	0 5	0 7	1 6
11	?12	?13	?15	?14
10	1 8	0 9	011	010

C1i = C1i-1 Xi' + C2i-1' C1i-1' Xi + C2i-1' C0i-1 Xi' + C2i-1 C0i-1' Xi'
= C1i-1 Xi' + C2i-1' C1i-1' Xi + Xi' (C2i-1 ⊕ C0i-1)

	00	01	11	10
00	0 0	0 1	0 3	0 2
01	0 4	1 5	1 7	0 6
11	?12	?13	?15	?14
10	0 8	1 9	111	110

C2i = C1i-1 Xi + C2i-1 Xi + C2i-1 C0i-1

(iv) Write a Verilog model for modeling your 1-bit cell by using an assign statement for each output.

```
module OneCell (output C2i, C1i, C0i, Zi, input C2i_1, C1i_1, C0i_1, Xi);

assign Zi = C0i_1 ~^  Xi;

assign C0i = C1i_1 ^ (~C0i_1 |  Xi);

assign C1i = C1i_1 & ~Xi | ~C2i_1 &  ~C1i_1 & Xi | ~Xi &  (C2i_1 ^ C0i_1);

assign C2i = C1i_1 & Xi | C2i_1 & Xi | C2i_1 & C0i_1;

endmodule
```

(v) Write a Verilog model for modeling a 4-bit circuit based on the 1-bit model you have.

```
module D3XM3 (output C2, C1, C0, output [3:0] Z, input [3:0] X);
```

```
OneCell M1 (C2_0, C1_0, C0_0, Z[0],0, 0, 0, X[0]);
OneCell M2 (C2_1, C1_1, C0_1, Z[1],C2_0, C1_0, C0_0, X[1]);
OneCell M3 (C2_2, C1_2, C0_2, Z[2],C2_1, C1_1, C0_1, X[2]);
OneCell M4 (C2, C1, C0, Z[3],C2_2, C1_2, C0_2, X[3]);

endmodule
```

(vi) Write a Verilog test bench to test the correctness of your design for the following input values: {X=1}, {X=3}, {X=5} and {X=4}.

```
module D3XM3_Test();

reg [3:0] X;
wire C2, C1, C0;
wire [3:0] Z;

D3XM3 M1 (C2, C1, C0, Z, X);

initial begin

X=4'b0001;

#100 X=4'b0011;

#100 X=4'b0101;

#100 X=4'b0100;

end

endmodule
```

The generated simulation waveform verifies the correct functionality of the designed circuit: