COE 405, Term 162

Design & Modeling of Digital Systems

Assignment# 1

Due date: Saturday, March 4

Q.1. Consider the two functions f=(a ⊕ b) + (a ⊕ c) and g=a b + a' c + b' c'.

(i) Implement the function f using only 2x1 MUXs and inverters minimizing the number of MUXs used.

(ii) Compute the function f⊕g based on orthonormal basis expansion.

Q.2. It is required to design an iterative combinational circuit that computes the equation Z=3*X-3, where X is an n-bit unsigned number.

(i) Determine the number of inputs and outputs needed for your 1-bit cell. Explain the meaning of values in the interface signals.

(ii) Derive the truth table of your 1-bit cell.

(iii) Derive minimized equations for your 1-bit using K-Map method.

(iv) Write a Verilog model for modeling your 1-bit cell by using an assign statement for each output.

(v) Write a Verilog model for modeling a 4-bit circuit based on the 1-bit model you have.

(vi) Write a Verilog test bench to test the correctness of your design for the following input values: {X=1}, {X=3}, {X=5} and {X=4}.

This assignment can be solved based on a group of two students. The solution should be well organized. Submit a soft copy of your solution in a zip file including your Verilog models. Your solution should be submitted in a PDF file that contains the following items:

i. Your name and ID

ii. Assignment number

iii. Problem statement

iv. Your solution

v. Include snapshots of simulation output to illustrate the correctness of your models.