Name: **Id#**

COE 301/ICS 233, Term 172

Computer Architecture & Assembly Language

Quiz# 7

Date: Tuesday, May 1, 2018

Q1. A benchmark program runs for 100 seconds. We want to improve the speedup of the benchmark by a factor of 3. We enhance the floating-point hardware to make floating point instructions run 5 times faster. How much of the initial execution time would floating-point instructions have to account for to show an overall speedup of 3 on this benchmark?

Q2. Consider the following fragment of MIPS code. Assume that **`a`** and **`b`** are arrays of words and the base address of **`a`** is in **`$a0`** and the base address of **`b`** is in **`$a1`**. How many instructions are executed during the running of this code? If ALU instructions (**addu** and **addiu**) take 1 cycle to execute, load/store **(lw** and **sw)** take 5 cycles to execute, and the branch (**bne**) instruction takes 3 cycles to execute, how many cycles are needed to execute the following code (all iterations). What is the average CPI?

```
            addu $t0, $zero, $zero   # i = 0
            addu $t1, $a0, $zero     # $t1 = address of a[i]
            addu $t2, $a1, $zero     # $t2 = address of b[i]
            addiu $t3, $zero, 101    # $t3 = 101 (max i)
loop:       lw $t4, 0($t2)           # $t4 = b[i]
            addu $t5, $t4, $s0       # $t5 = b[i] + c
            sw $t5, 0($t1)           # a[i] = b[i] + c
            addiu $t0, $t0, 1        # i++
            addiu $t1, $t1, 4        # address of next a[i]
            addiu $t2, $t2, 4        # address of next b[i]
            bne $t0, $t3, loop       # loop if (i != 101)
```

Q3. We want to compare the performance of a **single-cycle CPU design** with a **multicycle CPU**. Suppose we add the multiply and divide instructions. The operation times are as follows:

Instruction memory access time = 190 ps,	Data memory access time = 190 ps
Register file read access time = 150 ps,	Register file write access = 150 ps
ALU delay for basic instructions = 190 ps,	Delay for multiply or divide = 550 ps

Ignore the other delays in the multiplexers, control unit, sign-extension, etc.

Assume the following instruction mix: 30% ALU, 15% multiply & divide, 30% load & store, 15% branch, and 10% jump.

i. What is the total delay for each instruction class and the clock cycle for the single-cycle CPU design?

ii. Assume we fix the clock cycle to 200 ps for a multi-cycle CPU, what is the CPI for each instruction class and the speedup over a fixed-length clock cycle? Note that this implies that multiply and divide operations will be performed in multiple cycles.