Name: **Id#**

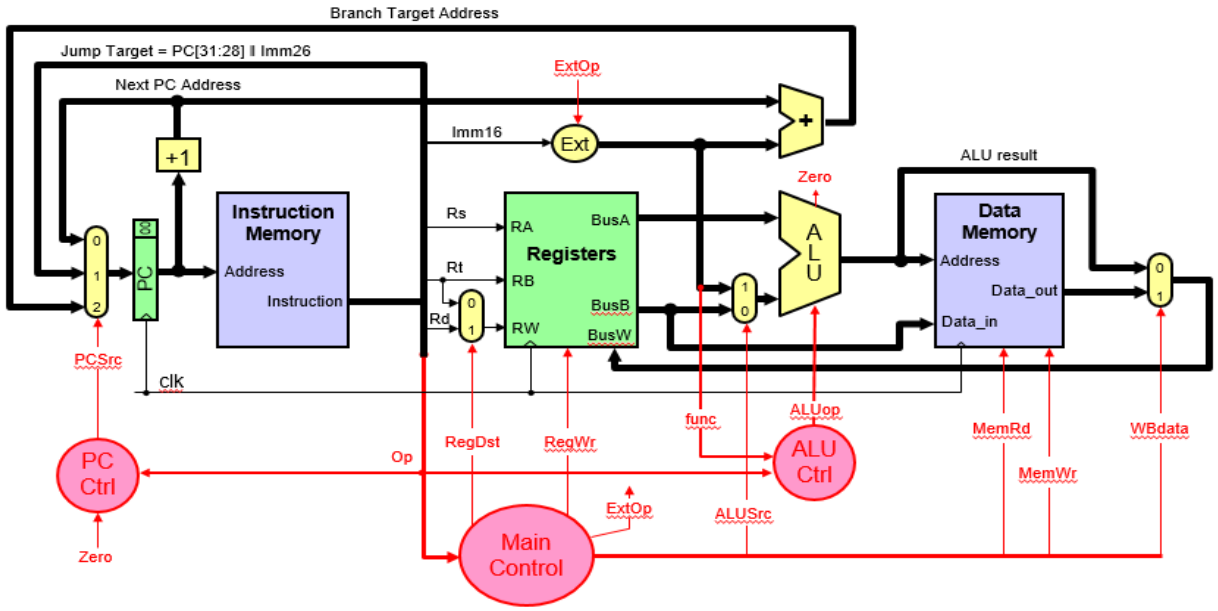
COE 301/ICS 233, Term 172

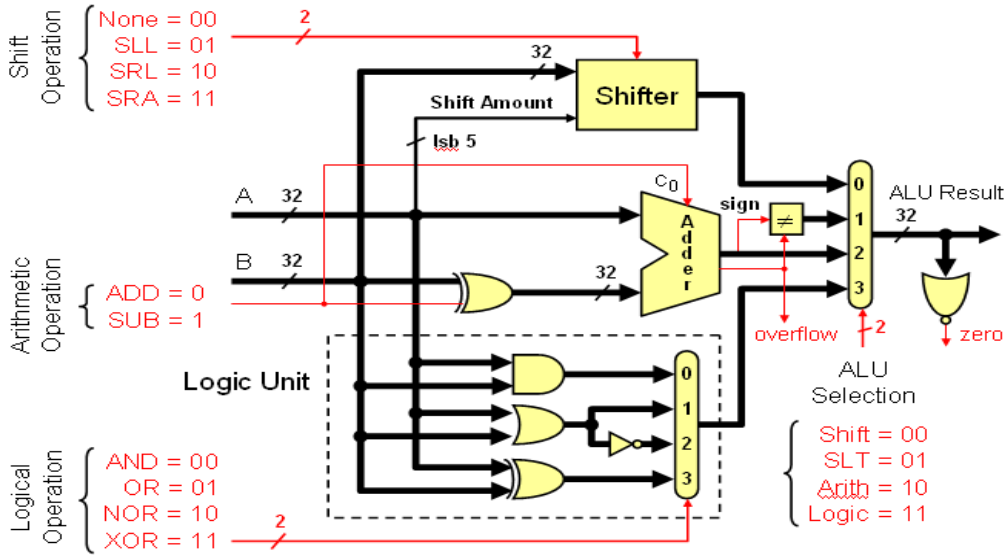
Computer Architecture & Assembly Language

Quiz# 6

Date: Tuesday, April 17, 2018

Q1. Consider the single-cycle datapath and control given below along with ALU design for the MIPS processor implementing a subset of the instruction set:





(i) **(5 points)** Show the control signals generated for the execution of the following instructions by filling the table given below:

Op	RegDst	RegWrite	ExtOp	ALUSrc	MemRead	MemWrite	WBdata
R-type							
xori							
lw							
bne							
j							

(ii) **(4 points)** Show the block diagram for designing the main control unit for this CPU and show the logic gates or equations for the control signals **RegDst**, **RegWrite** and **ExtOp** based on these instructions. Assume that the opcode of these instructions is a 6-bit opcode such that the opcode for R-type instructions is 0, the opcode for xori is 1, the opcode for lw is 2, and so on for the rest of the instructions.

(iii) **(12 points)** We wish to add the following instructions to the MIPS single-cycle datapath. Add any necessary datapath modifications and control signals needed for the implementation of these instructions. Show only the **modified** and **added** components to the datapath.

a. srl

b. lui

c. bgtz

d. jal