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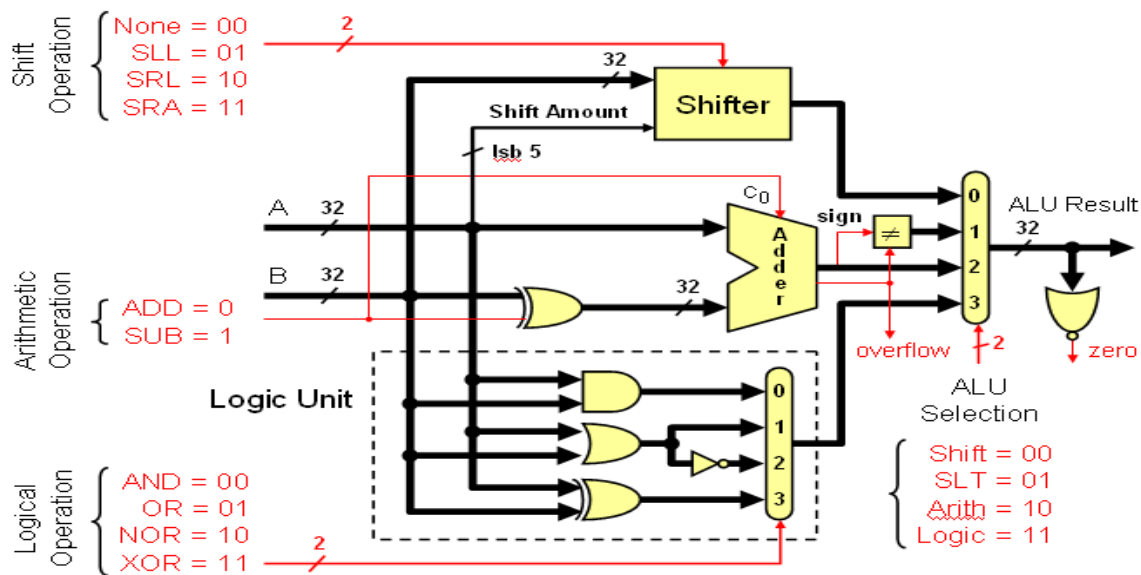
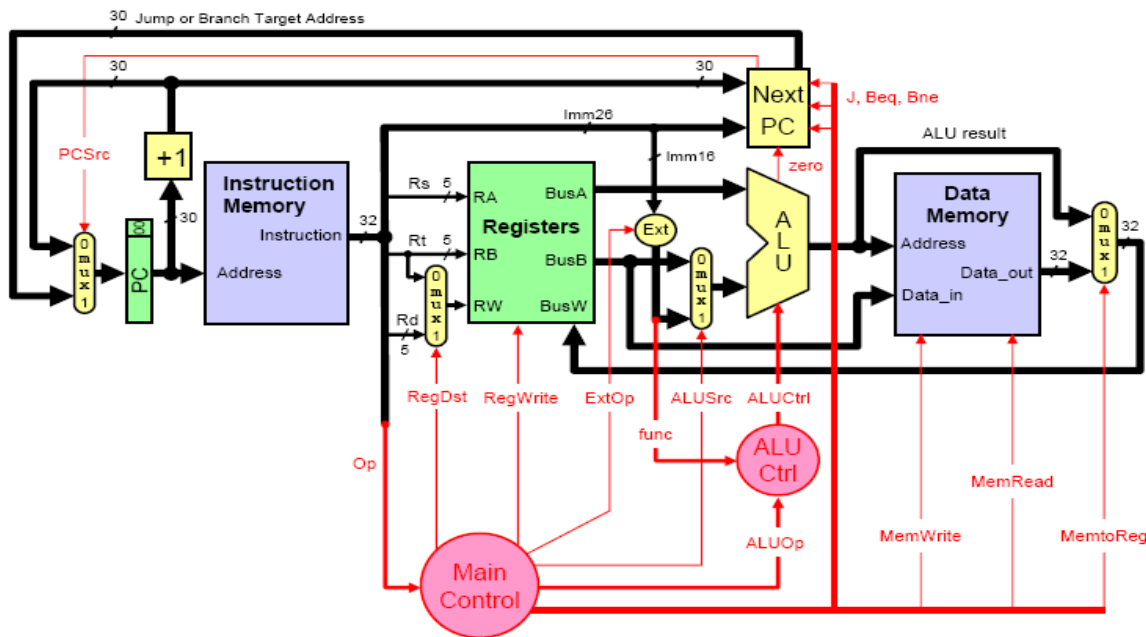
ICS 233, Term 141

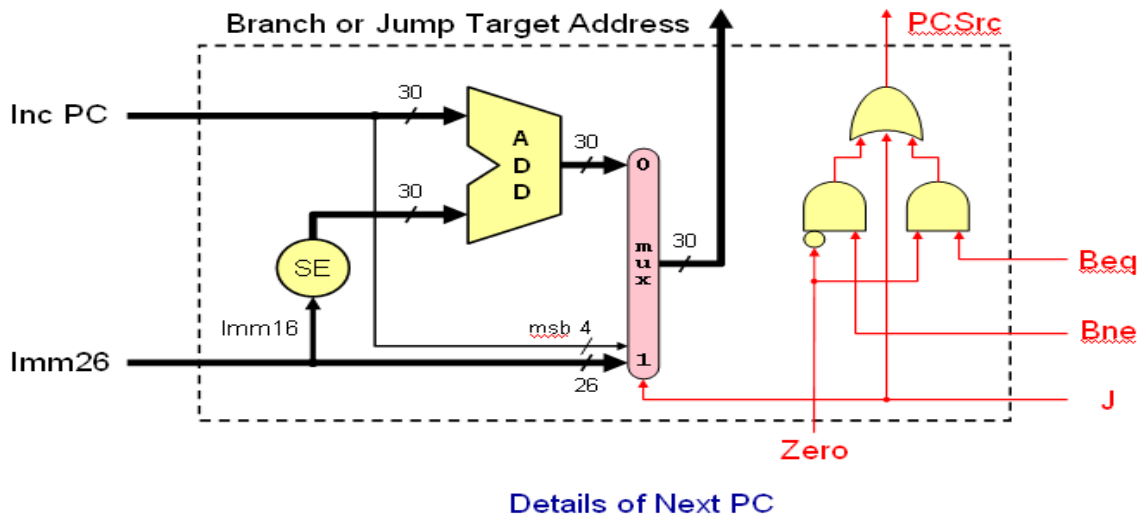
Computer Architecture & Assembly Language

Quiz# 6

Date: Monday, Dec. 22, 2014

Q1. Consider the single-cycle datapath and control given below along with ALU and Next PC blocks design for the MIPS processor implementing a subset of the instruction set:





(i) Show the control signals generated for the execution of the following instructions by filling the table given below:

Op	RegDst	RegWrite	ExtOp	ALUSrc	ALUOp	Beq	Bne	J	MemRead	MemWrite	MemtoReg
R-type											
xori											
lw											
bne											

The format of these instructions is given below for your reference:

Instruction	Meaning	Format
sub rd, rs, rt	$rd = rs - rt$	$Op^6 = 0$ rs ⁵ rt ⁵ rd ⁵ 0 0x22
xori rt, rs, imm ¹⁶	$rt = rs \wedge imm^{16}$	0x0e rs ⁵ rt ⁵ imm ¹⁶
lw rt, imm ¹⁶ (rs)	$rt = MEM[rs+imm^{16}]$	0x23 rs ⁵ rt ⁵ imm ¹⁶
bne rs, rt, label	branch if (rs != rt)	0x05 rs ⁵ rt ⁵ imm ¹⁶

(ii) We wish to add the following instructions to the MIPS single-cycle datapath. Add any necessary datapath modifications and control signals needed for the implementation of these instructions. Show only the **modified** and **added** components to the datapath. Show the values of the control signals to control the execution of each instruction.

a. lui

Instruction	Meaning	Format
lui rt, imm ¹⁶	$rt = imm^{16} \ll 16$	$Op^6 = 0xf$ 0 rt ⁵ imm ¹⁶

b. sltiu

Instruction		Meaning	Format			
sltiu	rt, rs, imm ¹⁶	rt=(rs<imm?1:0)	Op ⁶ = 0xb	rs ⁵	rt ⁵	imm ¹⁶

c. bgtz

Instruction		Meaning	Format			
bgtz	rs, label	branch if (rs>0)	Op ⁶ = 7	rs ⁵	0	imm ¹⁶

(iii) Assume that the propagation delays for the major components used in the datapath are as follows:

- Instruction and data memories: 150 ps
- ALU and adders: 100 ps
- Register file access (read or write): 60 ps
- Main control: 20 ps
- ALU control: 20 ps

Ignore the delays in the multiplexers, PC access, extension logic, and wires. What is the cycle time for the single-cycle datapath given above?

