Name: Id#

COE 301/ICS 233, Term 171

Computer Architecture & Assembly Language

Quiz# 5

 Date: Tuesday, Nov. 28, 2017

# **Q1.** Consider the single-cycle datapath and control given below along with ALU design for the MIPS processor implementing a subset of the instruction set:



##

## Show the control signals generated for the execution of the following instructions by filling the table given below: **(5 points)**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Op | RegDst | RegWrite | ExtOp | ALUSrc | ALUOp | Beq | Bne | J | MemRead | MemWrite | MemtoReg |
| R-type |  |  |  |  |  |  |  |  |  |  |  |
| slti |  |  |  |  |  |  |  |  |  |  |  |
| sw |  |  |  |  |  |  |  |  |  |  |  |
| beq |  |  |  |  |  |  |  |  |  |  |  |
| j  |  |  |  |  |  |  |  |  |  |  |  |

## Excluding the ALUOp, Beq, Bne and J signals, show the design of the control unit for the control signals given in the table above based on the given instructions. Assume that the opcode of these instructions is a 6-bit opcode such that the opcode for R-type instructions is 0, the opcode for slti is 1, the opcode for sw is 2, and so on for the rest of the instructions. **(5 points)**

## Show the design of the Next PC block. **(4 points)**

## We wish to add the following instructions to the MIPS single-cycle datapath. Add any necessary datapath modifications and control signals needed for the implementation of these instructions. Show only the **modified** and **added** components to the datapath.

* 1. sra **(3 points)**

|  |  |  |
| --- | --- | --- |
| Instruction | Meaning | Format |
|  sra rd, rt, imm5 |  rd= rt>>imm16 | Op6 = 0 | 0 | rt5 | rd5 | Imm5 | f6=3 |

* 1. jr **(3 points)**

|  |  |  |
| --- | --- | --- |
| Instruction | Meaning | Format |
|  jr rs |  PC=rs | op6 = 0 | rs5 | 0 | 0 | 0 | 8 |

## Assume that the propagation delays for the major components used in the datapath are as follows:

* + - Instruction and data memories: 120 ps
		- ALU and adders: 30 ps
		- Register file access (read or write): 14 ps
		- Main control: 8 ps
		- ALU control: 7 ps

Ignore the delays in the multiplexers, PC access, extension logic, and wires. What is the cycle time for the single-cycle datapath given above? **(3 points)**