

Name:

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**COE 301/ICS 233, Term 172**

**Computer Architecture & Assembly Language**

**Quiz# 3 Solution**

Date: Thursday, March 1, 2018

**Q1.** Fill in the blank in each of the following questions:

- (1) The pseudo instruction *ble \$s2, \$s1, Next* is implemented by the following minimum MIPS instructions:

slt \$at, \$s1, \$s2  
beq \$at, \$0, Next

- (2) Assume that the instruction *bne \$t0, \$t1, NEXT* is at address 0x00400020 in the text segment, and the label NEXT is at address 0x00400010. Then, the address stored in the assembled instruction for the label NEXT is (0x00400010-(0x00400020+4))/4=0xffffb.

- (3) Assuming that variable Array is defined as shown below:

Array: .byte 1, 2, -3, 4

After executing the following sequence of instructions, the content of the three registers is \$t1=0xffffffff, \$t2=0x000004fd and \$t3=0x04fd0201.

la \$t0, Array  
lb \$t1, 2(\$t0)  
lh \$t2, 2(\$t0)  
lw \$t3, 0(\$t0)

- (4) The content of register **\$t0** after executing the following code is 1+2+3+4=0xa:

li \$s1, 0x4321  
xor \$t0, \$t0, \$t0  
Next:  
andi \$t1, \$s1, 0xf  
add \$t0, \$t0, \$t1  
srl \$s1, \$s1, 4  
bne \$s1, \$0, Next

**Q2.** Write a MIPS assembly fragment for the following IF statement:

**if ( [(a == b) || ( c== d) ] && (a < c) ) then b = d ;**

Assume that variables a, b, c, and d are stored into registers \$s0, \$s1, \$s2, and \$s3, respectively.

```
                                bge $s0, $s2, exit
                                beq $s0,$s1, process
                                bne $s2, $s3, exit
process:                       Add $s1, $s3, $zero
Exit:
```

**Q3.** Write a MIPS assembly fragment for displaying the binary content of register \$s0. Note that the system call for printing a an integer in \$a0 sets \$v0 to 1.

```
# Initializing loop counter $t3
    li $t3, 32
loop:
    rol $s0, $s0, 1
    andi $a0,$s0, 1
# Print the integer result in a0
    li $v0, 1          # Load the system call number
    syscall
    subi $t3, $t3, 1
    bne $t3, $zero, loop
```