Name: **Id#**

ICS 233, Term 142

Computer Architecture & Assembly Language

Quiz# 2

Date: Tuesday, Feb. 24, 2015

Q1. Fill in the blank in each of the following questions:

(1) Assuming that variable Array is defined as shown below:

Array: .byte 1, -1, 2, -2, 3, -3, 4, -4

After executing the following sequence of instructions, the content of the three registers is $t1=_____, $t2=_____, and $t3=_____.

```
la $t0, Array
lbu $t1, 4($t0)
lh $t2, 4($t0)
lw $t3, 4($t0)
```

(2) Assume that the instruction j NEXT is at address 0x0040002c in the text segment, and the label NEXT is at address 0x00400018. Then, the address stored in the assembled instruction for the label NEXT is _____.

(3) Assume that the instruction bne $t0, $t1, NEXT is at address 0x0040002c in the text segment, and the label NEXT is at address 0x00400018. Then, the address stored in the assembled instruction for the label NEXT is _____.

(4) Assuming that $a0 contains an Alphabetic character, the instruction _____ will guarantee that the character in $a0 is always an lower case character. Note that the ASCII code of character 'A' is 0x41 while that of character 'a' is 0x61.

(5) The pseudo instruction bge $s2, $s1, Next is implemented by the following minimum native MIPS instructions:

_____

_____

(6) To multiply the signed content of register $t0 by 48.25 without using multiplications and division instructions, we use the following instructions:

_____

_____

_____

_____

_____

Q2. Write a MIPS assembly code fragment with minimum instructions to implement the following high level language code structure:

```
i = 0;
size = 10;
while (i < size && A[i] !=0){
     A[i] = A[i + 1] ;
     i = i + 1;
 }
```

Assume that the assembler has assigned `i` to register `$s0`, `size` to register `$s1`, and has stored the address of array `A` in register `$s2`. Assume that `A` is an array of integers.