Name: KEY **Id#**

ICS 233, Term 063

Computer Architecture & Assembly Language

Quiz# 1

Date: Saturday, July 14, 2007

Q1. Fill the blanks in the following questions:

1. Assuming **6-bit 2`s complement** representation, the smallest (negative) number is **100000** in binary and **-32** in decimal and the largest (positive) number is **011111** in binary and **+31** in decimal**.**

2. Consider an **8-bit** register that has the binary number 10110100. The decimal value of this number as a signed number in sign-magnitude representation is **-52** while in 1's complement representation it is **-75** and in 2's complement representation it is **-76**.

3. Assuming **8-bit 2`s complement** representation, the number F0 represents the decimal number **-16**.

4. The binary number 01100100 represents character **d**, **and** uses an **odd** parity bit. Note that the ASCII code of character **A** is 41H and that of character **a** is 61H.

5. The **Program Counter** register is the register in the CPU that holds the address of the next instruction to be fetched from memory.

6. The **Instruction** register is the register in the CPU that stores the machine language instructions, temporarily, after the instructions are fetched from memory.

7. Given that a wafer can be diced into 2000 dies, out of which 800 dies are defective. Then, the yield is **(2000-800)/2000=1200/2000=60%**.
8. Given a magnetic disk with Rotation speed = 7200 RPM (rotations per minute). Then, the average rotation latency, i.e. time to locate needed sector is **0.5*1000*60/7200=4.17 ms**.

9. **The Instruction Set Architecture** is a specific interface that the hardware provides the low-level software which includes the instruction set, programmer accessible registers and memory.
10. **Cache** is a small fast memory that acts as a buffer for the main memory.

11. **Operating System** is a program that manages the resources of a computer for the benefit of the programs that run on that machine.

12. **Assembler** is a program that converts symbolic versions of instructions into their binary formats.

13. **Datapath** is component of the processor that performs arithmetic operations.

14. Given and address bus of 32 bits and data bus of 32 bits, the maximum memory size that can be interfaced with the CPU is $\mathbf{2^{32}=4G}$ bytes and the maximum number of bytes that can be read in a single read/write cycle is **32/8=4** bytes.

Q2. Perform the following arithmetic operations assuming that numbers are represented using **8-bit 2's complement** representation. Indicate in your answer when an *overflow* occurs.

i. FC + AF

= AB

There is **no overflow** as adding two negative numbers produced a negative number.

ii. 81 – 7D

= 81 + 83 = 04

There is **overflow** as adding two negative numbers produced a positive number.