Name: Id#

COE 301/ICS 233, Term 161

Computer Architecture & Assembly Language

Quiz# 1

Date: Tuesday, Oct. 11, 2016

# **Q1.** Fill the blanks in the following questions:

## Assuming 12-bit unsigned representation, the binary number 1111 0000 1111 is equal to the decimal number \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Assuming 12-bit signed 2`s complement representation, the hexadecimal number FC0 is equal to the decimal number \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ is a register that holds the address of the next instruction to be fetched from memory.

## Two main advantages of programming in high-level language are: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Two main advantages of programming in assembly language are: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## With a 36-bit address bus and 64-bit data bus, the maximum memory size (assuming byte addressable memory) that can be accessed by a processor is \_\_\_\_\_\_\_\_\_\_\_ and the maximum number of bytes that can be read or written in a single cycle is \_\_\_\_\_\_\_\_\_\_\_\_.

## The bandwidth mismatch between the speed of processor and the speed of main-memory is alleviated by using \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## The advantage of dynamic RAM over static RAM is that it is \_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_ but the disadvantage is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## The instruction set architecture of a processor consists of \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Assuming that the CPU has just read a 32-bit MIPS instruction from the address 0x00400008, then, the address of the next instruction that this CPU is going to read is\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Given a magnetic disk with the following properties:

* Time of one rotation is 8 ms
* Average seek = 8 ms, Sector = 512 bytes, Track = 200 sectors

The average time to access a block of 20 consecutive sectors is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ms.