KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

ICS 233 Computer Architecture & Assembly Language
Syllabus - Term 142

Catalog Description

Machine organization; assembly language: addressing, stacks, argument passing, arithmetic operations, decisions, modularization; input/output operations and interrupts; memory hierarchy and cache memory; datapath design; pipeline design techniques.

Prerequisite: COE 202 and ICS 201

Instructor Dr. Aiman H. El-Maleh. Room: 22/407-5 Phone: 2811
Email: aimane@kfupm.edu.sa

Office Hours UTWR 12:15-1:00 PM, M 11:00-12:00 PM, and by appointment

Text Books

- David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware /Software Interface*, Fifth Edition, Morgan Kauffmann Publishers, 2013.

Course Objectives

1. Expose students to the trade-off analysis in designing various aspects of computer architecture, which includes processor design, instruction set design, memory hierarchy, and instruction level pipelining.
2. To provide students with intermediate level experience in assembly language programming.

Course Learning Outcomes

Upon completion of the course, you should have the ability to:

For Course Objective 1:

1. Analyze, write, and test MIPS assembly language programs. [LO c]
2. Describe the organization and operation of integer and floating-point arithmetic units. [LO a]
3. Apply the knowledge of mathematics to processor performance analysis. [LO a]
4. Design the datapath and control of a processor. [LO c]

For Course Objective 2:

5. Describe the memory hierarchy and caches. [LO a]
6. Use software tools for assembly language programming and for CPU design and simulation. [LO i]

Grading Policy

Discussions & Reflections	5%	
Programming Assignments	10%	
Quizzes	10%	
Major Exam I	15%	**(Sat., Feb. 28, 1:00 PM)**
Major Exam II	20%	**(Sun., April 19, 7:30 PM)**
Laboratory	10%	
Project	10%	
Final	20%	

- Attendance will be taken regularly.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted (upto 3 days) but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 10%.
- No makeup will be made for missing Quizzes or Exams.

Course Topics

1. ***Introduction***
   Introduction to computer architecture, assembly and machine languages, components of a computer system, memory hierarchy, instruction execution cycle, chip manufacturing process, technology trends, programmer's view of a computer system.
2. ***Review of Data Representation***
   Binary and hexadecimal numbers, signed integers, binary and hexadecimal addition and subtraction, carry and overflow, characters and ASCII table.
3. ***Instruction Set Architecture***
   Instruction set design, RISC design principles, MIPS instructions and formats, registers, arithmetic instructions, bit manipulation, load and store instructions, byte ordering, jump and conditional branch instructions, addressing modes, pseudo instructions.
4. ***MIPS Assembly Language Programming***
   Assembly language tools, program template, directives, text, data, and stack segments, defining data, arrays, and strings, array indexing and traversal, translating expressions, if else statements, loops, indirect jump and jump table, console input and output.
5. ***Procedures and the Runtime Stack***
   Runtime stack and its applications, defining a procedure, procedure calls and return address, nested procedure calls, passing arguments in registers and on the stack, stack frames, value and reference parameters, saving and restoring registers, local variables on the stack.
6. ***Interrupts***
   Software exceptions, syscall instruction, hardware interrupts, interrupt processing and handler, MIPS coprocessor 0.
7. ***Integer Arithmetic and ALU design***
   Hardware adders, barrel shifter, multifunction ALU design, integer multiplication, shift add multiplication hardware, Shift-subtract division algorithm and hardware, MIPS integer multiply and divide instructions, HI and LO registers.
8. ***Floating-point arithmetic***

Floating-point representation, IEEE 754 standard, FP addition and multiplication, rounding, MIPS floating-point coprocessor and instructions.

9. ***CPU Performance***
   CPU performance and metrics, CPI and performance equation, MIPS, Amdahl's law.

10. ***Single-Cycle Datapath and Control Design***
    Designing a processor, register transfer, datapath components, register file design, clocking methodology, control signals, implementing the control unit, estimating longest delay.

11. ***Pipelined Datapath and Control***
    Pipelining concepts, timing and performance, 5-stage MIPS pipeline, pipelined datapath and control, pipeline hazards, data hazards and forwarding, control hazards, branch prediction.

12. ***Memory System Design***
    Memory hierarchy, SRAM, DRAM, pipelined and interleaved memory, cache memory and locality of reference, cache memory organization, write policy, write buffer, cache replacement, cache performance, two-level cache memory.