KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

ICS 233 Computer Architecture & Assembly Language
Syllabus - Term 081

Catalog Description

Machine organization; assembly language: addressing, stacks, argument passing, arithmetic operations, decisions, modularization; Input/Output Operations and Interrupts; Memory Hierarchy and Cache memory; Pipeline Design Techniques; Super-scalar architecture; Parallel Architectures.

Prerequisite: COE 202 and ICS 201

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Office Hours SUMT 1:00-2:00 PM, and by appointment

Text Books

- David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware /Software Interface*, Third Edition, Morgan Kauffmann Publishers, 2005.
- Robert L. Britton, *MIPS Assembly Language Programming*, Pearson Prentice Hall, 2004.

Course Objectives

After successfully completing the course, students will be able to:

1. Describe the instruction set architecture of a MIPS processor.
2. Analyze, write, and test MIPS assembly language programs.
3. Describe the organization/operation of integer & floating-point arithmetic units.
4. Design the datapath and control of a single-cycle CPU.
5. Design the datapath/control of a pipelined CPU and handle hazards.
6. Describe the organization/operation of memory and caches.
7. Analyze the performance of processors and caches.

Course Learning Outcomes

1. Ability to analyze, write, and test MIPS assembly language programs.
2. Ability to describe the organization and operation of integer and floating-point arithmetic units.
3. Ability to apply knowledge of mathematics in CPU performance analysis and in speedup computation.
4. Ability to design the datapath and control unit of a processor.
5. Ability to use simulator tools in the analysis of assembly language programs and in CPU design.

Grading Policy

Discussions & Reflections	5%	
Programming Assignments	10%	
Quizzes	10%	
Exam I	15%	**(Th., Nov. 13, 1:00 PM)**
Exam II	15%	**(Th., Jan. 8, 1:00 PM)**
Laboratory	15%	
Project	10%	
Final	20%	

- Attendance will be taken regularly.
- Excuses for officially authorized absences must be presented no later than one week following resumption of class attendance.
- Late assignments will be accepted (upto 3 days) but you will be penalized 10% per each late day.
- A student caught cheating in any of the assignments will get 0 out of 10%.
- No makeup will be made for missing Quizzes or Exams.

Course Topics

1. ***Introduction***
   Introduction to computer architecture, assembly and machine languages, components of a computer system, memory hierarchy, instruction execution cycle, chip manufacturing process, technology trends, programmer's view of a computer system.
2. ***Review of Data Representation***
   Binary and hexadecimal numbers, signed integers, binary and hexadecimal addition and subtraction, carry and overflow, characters and ASCII table.
3. ***Instruction Set Architecture***
   Instruction set design, RISC design principles, MIPS instructions and formats, registers, arithmetic instructions, bit manipulation, load and store instructions, byte ordering, jump and conditional branch instructions, addressing modes, pseudo instructions.
4. ***MIPS Assembly Language Programming***
   Assembly language tools, program template, directives, text, data, and stack segments, defining data, arrays, and strings, array indexing and traversal, translating expressions, if else statements, loops, indirect jump and jump table, console input and output.

5. ***Procedures and the Runtime Stack***
   Runtime stack and its applications, defining a procedure, procedure calls and return address, nested procedure calls, passing arguments in registers and on the stack, stack frames, value and reference parameters, saving and restoring registers, local variables on the stack.

6. ***Interrupts***
   Software exceptions, syscall instruction, hardware interrupts, interrupt processing and handler, MIPS coprocessor 0.

7. ***Integer Arithmetic and ALU design***
   Hardware adders, barrel shifter, multifunction ALU design, integer multiplication, shift add multiplication hardware, Shift-subtract division algorithm and hardware, MIPS integer multiply and divide instructions, HI and LO registers.

8. ***Floating-point arithmetic***
   Floating-point representation, IEEE 754 standard, FP addition and multiplication, rounding, MIPS floating-point coprocessor and instructions.

9. ***CPU Performance***
   CPU performance and metrics, CPI and performance equation, MIPS, Amdahl's law.

10. ***Single-Cycle Datapath and Control Design***
    Designing a processor, register transfer, datapath components, register file design, clocking methodology, control signals, implementing the control unit, estimating longest delay.

11. ***Pipelined Datapath and Control***
    Pipelining concepts, timing and performance, 5-stage MIPS pipeline, pipelined datapath and control, pipeline hazards, data hazards and forwarding, control hazards, branch prediction.

12. ***Memory System Design***
    Memory hierarchy, SRAM, DRAM, pipelined and interleaved memory, cache memory and locality of reference, cache memory organization, write policy, write buffer, cache replacement, cache performance, two-level cache memory.