ICS DEPARTMENT

ICS 233

COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE

Midterm Exam

First Semester (141)

Time: 1:00-3:30 PM

Student Name : _KEY_____

Student ID. : _____

Question	Max Points	Score
Q1	35	
Q2	7	
Q3	20	
Q4	18	
Q5	10	
Q6	10	
Total	100	

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(Q1) Fill in the blank in each of the following questions:

- (1) Each memory cell of DRAM holds 1 bit of information and consists of <u>one</u> transistor(s) and <u>one</u> capacitor(s). (1 Point)
- (2) Typically, the SRAM technology is used for the <u>cache</u> memory. (1 Point)
- (3) Given a magnetic disk with rotation speed = 15000 rotations per minute and average seek time 10 milliseconds, then the time needed for one rotation is $\underline{60/15000=0.004s=4}$ milliseconds. (1 Point)
- (4) A processor with 2.0 GHz speed has a $1/(2x10^9)=0.5x10^{-9}s=500x10^{-12}s=500$ picoseconds clock cycle duration. (1 Point)
- (5) A certain chip manufacturing process produces 25 bad dies, on average. Given that the total number of dies on any given wafer is 300, then, this process has a yield equal to (300-25)/300=275/300=91.67 %. (1 Point)
- (6) Cache memory is faster than <u>random access</u> memory and slower than <u>registers</u>. (1 Point)
- (7) One main advantage for programming in high-level language is program development is faster or programs are portable.

(1 Point)

(8) One main advantage for programming in assembly language is <u>space and time</u> <u>efficiency</u> or <u>accessibility to system hardware.</u>

(1 Point)

(9) Assuming variable Array is defined as shown below:

Array: .byte 1, -1, 2, -2, 3, -3, 4, -4

After executing the following sequence of instructions, the content of the three registers is $t_{=0x0000003}$ $t_{=0xfffffd03}$ and $t_{=0xfc04fd03}$.

(3 Points)

la \$t0, Array lbu \$t1, 4(\$t0) lh \$t2, 4(\$t0) lw \$t3, 4(\$t0)

- (10) Assume that the instruction j NEXT is at address 0x0040002c in the text segment, and the label NEXT is at address 0x00400018. Then, the address stored in the assembled instruction for the label NEXT is 0x0100006. (2 Point)
- (11) Assume that the instruction bne \$t0, \$t1, NEXT is at address 0x0040002c in the text segment, and the label NEXT is at address 0x00400018. Then, the address stored in the assembled instruction for the label NEXT is (0x00400018-0x00400030)/4=0xfffa.
- (12) Given that the instruction jal MyProc is at address 0x0040002c in the text segment, and that MyProc is at address 0x00400018. Then, the address stored in \$ra register after executing this instruction is 0x00400030.

(1 Point)

(13) To allocate 10 words, each initialized by 0, we use the following assembler directive <u>.word 0:10</u>.

(1 Point)

(14) The pseudo instruction bge \$s2, \$s1, Next is implemented by the following minimum MIPS instructions:
<u>slt \$at, \$s2, \$s1</u>
<u>beq \$at, \$0, Next</u>

(2 Points)

(15) The code given below prints the following: <u>Midterm Exam</u> ICS 233 is easy!!

Note that the ASCII code for the line feed character is 10 and the ASCII code for the carriage return character is 13. (2 Points)

MSG: .ascii "Midterm Exam" .byte 10 .ascii "ICS 233 " .asciiz "is easy !! "

li \$v0, 4 la \$a0, MSG syscall (16) Using minimum native MIPS instructions, the assembly code to Jump to label L1 if bits 0, 2, and 5 in \$t0 are all set (i.e. =1) is:
ori \$t1 \$0, 0x25 andi \$t0, \$t0, \$t1 beq \$t0, \$t1, L1

(3 points)

(17) To multiply the signed content of register \$t0 by 63.75 without using multiplications and division instructions, we use the following instructions:
<u>sll \$t1, \$t0, 6</u>
<u>sra \$t2, \$t0, 2</u>
<u>subu \$t0, \$t1, \$t2</u>

(3 points)

(18) Assuming that all registers contain signed numbers, the MIPS assembly code (with minimum execution time) to implement the equation \$v0=(5-16*\$a0)/(\$a1) is :

<u>ori \$v0, \$0, 5</u> <u>shl \$t0, \$a0, 4</u> <u>subu \$v0, \$v0. \$t0</u> <u>div \$v0, \$a1</u> <u>mflo \$v0</u>

(3 points)

(19) Suppose that we would like to translate 8-bit numbers into characters according to a given translation table. Part of the translation table is shown below. The MIPS assembly code to translate a number in register \$t0 according to the translation table below and store the resulting character in the same register is (e.g. if \$t0=3 the program should store 'G' in \$t0):

0	1	2	3	4	5	6	7	8	
ʻa'	ʻC'	ʻx'	'G'	'y'	ʻ!'	'h'	'?'	'_'	

<u>.data Table .ascii "aCxGy!h?-"</u> <u>la \$t1, Table</u> <u>add \$t0, \$t0, \$t1</u> <u>lb \$t0, 0(\$t0)</u>

(2 points)

(20) Consider a simplified 5-bit floating-point representation following the general guidelines of the IEEE standard format. Suppose that the number of bits used for the exponent is 2 bits and for the fraction is 2 bits. Then, the smallest and largest positive values of normalized numbers that can be represented using this representation are $1.00x2^{0}=1$ and $1.11x2^{1}=14/4=3.5$ and the largest error in this representation is 0.25. (3 points)

(Q2)

(i) Assuming that <u>one byte is typed into each small block</u> (one word per row) in the table below, fill out the table for the following data segment. Assume a Little Endian ordering, which is the same as the Mars 4.4 simulator default. Start from the top and work out the rest of the memory segment. Assume that the address of the first byte is 0x10010000. Remember that hex numbers start with 0x. Note that you do not need to show the ASCII code of characters. (5 Points)

.data

var1:	.BYTE	3,'1', -7
.ALIGN	0	
var2:	.WORD	10
str1:	.ASCIIZ	"ICS"
.ALIGN	2	
var3:	.WORD	0xabcdef22
.ALIGN	3	
Var4:	.HALF	-1

MSB			LSB	Address
0a	f9	'1'	03	0x10010000
ʻI'	00	00	00	0x10010004
	00	'S'	ʻC'	0x10010008
ab	cd	ef	22	0x1001000c
		ff	ff	0x10010010
				0x10010014

(ii) Fill out the symbol table, below, that corresponds to the data segment in Part (i), above. (2 Points)

Label	Address
var1	0x10010000
var2	0x10010003
str1	0x10010007
var3	0x1001000c
var4	0x10010010

(Q3) Answer the following questions. Show how you obtained your answer:

(i) Determine what will be displayed after executing the following code: (5 Points)

li \$a0, 23 li \$a1, 5 div \$a0, \$a1 mflo \$a0 li \$v0, 1 syscall li \$a0, '.' li \$v0, 11 syscall li \$t0, 10 mfhi \$t1 mul \$t1, \$t1, \$t0 div \$t1, \$a1 mflo \$a0 li \$v0, 1 syscall

The program will display 4.6 which is the result of dividing 23 by 5.

(ii) Given the following definition in the data segment:

Array: .word 0, 1, 2, 3, 4 .word 5, 6, 7, 8, 9 .word 10, 11, 12, 13, 14

Determine the content of Array after executing the following code: (5 Points) la \$t0, Array

li \$t1, 5 li \$t2, 20 addu \$t2, \$t2, \$t0 li \$t3, 40 addu \$t3, \$t3, \$t0 Next: lw \$t4, 0(\$t2) lw \$t5, 0(\$t3) sw \$t5, 0(\$t3) sw \$t5, 0(\$t2) addi \$t2, \$t2, 4 addi \$t3, \$t3, 4 addi \$t1, \$t1, -1 bnez \$t1 Next

The code will swap row 1 and row 2 in the array and the content of Array after executing the code will be:

Array: .word 0, 1, 2, 3, 4 .word 10, 11, 12, 13, 14 .word 5, 6, 7, 8, 9 (iii) Determine what will be displayed after executing the following code: (5 Points)

li \$t0, 0x1d76 andi \$a0, \$t0, 0x1f li \$v0, 1 syscall li \$a0, '-' li \$v0, 11 syscall srl \$t0, \$t0, 5 andi \$a0, \$t0, 0xf li \$v0, 1 syscall li \$a0, '-' li \$v0, 11 syscall srl \$t0, \$t0, 4 andi \$a0, \$t0, 0x3ff addu \$a0, \$a0, 2000 li \$v0, 1 syscall

The program will display 22-11-2014, which is the date of the exam!.

(iv) Given the following definition in the data segment: (5 Points)

TABLE: .asciiz "Emad Ali Anas"

Determine the content of TABLE after executing the following code:

```
li $t0, 'a'
li $a0, '*'
la $t1, TABLE
addi $t1, $t1, -1
Next: addi $t1, $t1, 1
lbu $t2, 0($t1)
beq $t2, $0, ENL
ori $t2, $t2, 0x20
bne $t2, $t0, Next
sb $a0, 0($t1)
j Next
```

ENL:

The program will replace all occurrences of 'a' and 'A' in Table by '*. Thus the content of TABLE will be:

TABLE: .asciiz "Em*d *li *n*s"

(Q4) Write separate MIPS assembly code fragments with minimum instructions to implement each of the given requirements.

(i) Given the following high level language code structure, write down the corresponding MIPS assembly language instructions: (6 Points)

```
i = 1;
size = 10;
while (i < size || A[i] !=0) {
    A[i] = A[i] + A[i - 1];
    i = i + 1;
}
```

Assume that the assembler has assigned i to register \$s0, size to register \$s1, and has stored the address of array A in register \$s2.

	li \$s0, 1
	li \$s1, 10
While:	sll \$t0, \$s0, 2
	addu \$t0, \$s2, \$t0
	lw \$t1, 0(\$t0)
	bne \$t1, \$0, WhileBody
	bge \$s0, \$s1, EndWhile
WhileBody:	$1w $t_2, -4($t_0)$
5	addu \$t1, \$t1, \$t2
	sw \$t1, 0(\$t0)
	addiu \$s0, \$s0, 1
	j While

EndWhile:

(ii) Assuming that functions F and G receive two arguments in \$a0 and \$a1 and return their results in \$v0, implement the function F given below saving needed registers on the stack. Save changed registers according to the assumed programming convention. (6 Points)

```
int F(int a, int b) {
                return a+G(b, G(a, b));
        }
F:
                $sp, $sp, -12
                                # frame = 12 bytes
       addiu
                $ra, 0($sp)
                                # save $ra
       SW
                                # save argument a
                $a0, 4($sp)
       SW
                                # save argument b
                $a1, 8($sp)
        SW
                G
                                \# call g(a,b)
       jal
                                # $a0 = b
                $a0, 8($sp)
       lw
                $a1, $v0
                                # $a1 = g(a,b)
       move
                                \# call g(b, g(a,b))
       jal
                G
                $a0, 4($sp)
       lw
                                # $a0 = a
                                # $v0 = a+G(b, G(a, b))
       addu
                $v0, $a0, $v0
       lw
                $ra, 0($sp)
                                # restore $ra
       addiu
                $sp, $sp, 12
                                # free stack frame
                $ra
                                # return to caller
       jr
```

(iii) Write a procedure that counts the number of even and odd integers that are input via a keyboard. The user will continue to enter nonnegative integers until he enters -1 to terminate the input. The procedure is called countevenodd and returns the total count of odd integers in register \$v1 and the total count of even integers in register \$v0. Assume that a main program prompts the user asking for input and that the main program will print the output counts with proper messages. You do not need to write the main program code. (6 Points)

Countevenodd:

xor \$t0, \$t0, \$t0	# number counter
xor \$v1, \$v1, \$v1	# odd counter
li \$v0, 5	
syscall	# read integer
beq \$v0, -1, EndLoop	
andi \$v0, \$v0, 1	
add \$v1, \$v1, \$v0	# count number of odd's
addi \$t0, \$t0, 1	
j Loop	
op:	
subu \$v0, \$t0, \$v1	# compute number of even
jr \$ra	L
	xor \$v1, \$v1, \$v1 li \$v0, 5 syscall beq \$v0, -1, EndLoop andi \$v0, \$v0, 1 add \$v1, \$v1, \$v0 addi \$t0, \$t0, 1 j Loop op: subu \$v0, \$t0, \$v1

(Q5)

(i) Assume that we have a **Multiplicand** = **1100** and a **Multiplier** = **0011**.

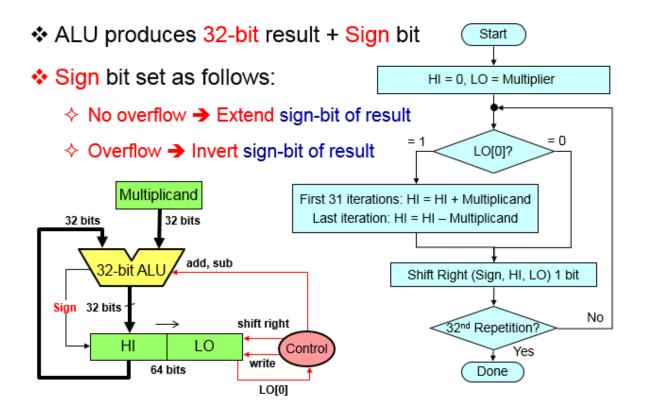
Using the revised unsigned multiplication hardware, show the unsigned multiplication product for the given numbers, above. The result of the multiplication should be an 8 bit unsigned number in the HI and LO registers. Show all the steps of your work.

(4 Points)

Ite	eration	Multiplicand	Carry	Product = HI,LO
0	Initialize	1100		00000011
1	$LO[0] = 1 \Rightarrow ADD$		0	11000011
	Shift Right Product = (HI, LO)			01100001
2	$LO[0] = 1 \Longrightarrow ADD$		1	00100001
	Shift Right Product = (HI, LO)			10010000
3	$LO[0] = 0 \Longrightarrow$ Do Nothing		0	10010000
	Shift Right Product = (HI, LO)			01001000
4	$LO[0] = 0 \Longrightarrow$ Do Nothing		0	01001000
	Shift Right Product = (HI, LO)			00100100

(ii) Show the hardware diagram that corresponds to the revised integer (signed) multiplication. <u>Carefully label all parts and connections</u> in your diagram.

(6 Points)



(Q6)

120.125=(1111000.001)₂ = (1.111000001)₂ * 2⁶ Exp. = 6 +127=133 Single precision binary representation: 0100 0010 1111 0000 0100 0000 0000

(iii) Perform the following floating-point operation rounding the result to the <u>nearest even</u>. Perform the operation using guard, round and sticky bits.

	1100	0001	1000	0000	0000	0000	0000	0100
+	0100	0011	1000	1000	0000	0000	0000	0000

(6 Points)

	1.000	1000	0000	0000	0000	0000	000	x 2 ⁸
-	1.000	0000	0000	0000	0000	0100	000	x 2 ⁴
=	1.000	1000	0000	0000	0000	0000	000	x 2 ⁸
-	0.000	1000	0000	0000	0000	0000	010	x 2 ⁸ (align)
=	01.000	1000	0000	0000	0000	0000	000	x 2 ⁸
+	11.111	0111	1111	1111	1111	1111	110	x 2 ⁸ (2's complement)
=	00.111	1111	1111	1111	1111	1111	110	x 2 ⁸
=	+0.111	1111	1111	1111	1111	1111	110	x 2 ⁸
=	+1.111	1111	1111	1111	1111	1111	100	x 2 ⁷ (normalize)

Next, we round to the nearest even by adding 1 and the result becomes:

= +10.000 0000 0000 0000 0000 x 2⁷ (round)

Next, we renormalize the result and the result becomes:

```
= +1.000 0000 0000 0000 0000 x 2<sup>8</sup> (renormalize)
```

Syscall Services:

Service	\$v0	Arguments / Result
Print Integer	1	\$a0 = integer value to print
Print Float	2	<pre>\$f12 = float value to print</pre>
Print Double	3	<pre>\$f12 = double value to print</pre>
Print String	4	\$a0 = address of null-terminated string
Read Integer	5	Return integer value in \$v0
Read Float	6	Return float value in \$f0
Read Double	7	Return double value in \$f0
Read String	8	<pre>\$a0 = address of input buffer \$a1 = maximum number of characters to read</pre>
Print Char	11	\$a0 = character to print
Read Char	12	Return character read in \$v0

MIPS Instructions:

add \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x20 addu \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x20 addu \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x20 subu \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x23 Instruction Meaning R-Type Format and \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x24 or \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x24 or \$s1, \$s2, \$s3 \$s1 = \$s2 + \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x24 rs \$s2, \$rd \$s1 \$s2 = \$rd \$s3 \$s1 = \$s2 + \$s1 \$s1 = \$s1 \$s1 = \$s2 s1 \$s2 rd = \$s1 \$s1 = \$s2 rd = \$s1 \$s1 = \$s2 rd = \$s1 \$s1 = \$s1	Inst	ruction	Meaning				R-T\	vpe F	orma	t	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				op =	= 0 rs =		_	_			f = 0x20
subu \$s1, \$s2, \$s3 \$s1 = \$s2 - \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x23 Instruction Meaning R-Type Format and \$s1, \$s2, \$s3 \$s1 = \$s2 & \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x23 and \$s1, \$s2, \$s3 \$s1 = \$s2 & \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x23 Instruction Meaning R-Type Format sa \$s1, \$s2, 10 \$s1 = \$s2 < rd = \$s1 sa = 0 f = 0x27 Instruction Meaning R-Type Format sil \$s1, \$s2, 10 \$s1 = \$s2 <<10 op = 0 rs = \$s1 sa = 0 f = 0 rs = \$s1, \$s2, 10 \$s1 = \$s2 <rd \$s1<="" th=""> \$s1 = \$s2 rd = \$s1 sa = 0 f = 0 <td>addu</td><td></td><td></td><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></rd>	addu			-							
Instruction Meaning R-Type Format and \$s1, \$s2, \$s3 \$s1 = \$s2 & \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x24 or \$s1, \$s2, \$s3 \$s1 = \$s2 & \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x26 or \$s1, \$s2, \$s3 \$s1 = \$s2 ^ \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x26 nor \$s1, \$s2, \$s3 \$s1 = \$s2 ^ \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x26 nor \$s1, \$s2, \$s3 \$s1 = \$s2 <<10	sub	\$s1, \$s2, \$s3	\$s1 = \$s2 - \$s3	op =	= 0 rs =	= \$s2	rt =	\$s3 rd	= \$s1	sa = 0	f = 0x22
and \$s1, \$s2, \$s3 \$s1 = \$s2 & \$s3 op = 0 rs = \$s2 rt = \$s3 rt = \$s1 sa = 0 f = 0x24 or \$s1, \$s2, \$s3 \$s1 = \$s2 \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x26 xor \$s1, \$s2, \$s3 \$s1 = \$s2 ^ \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x26 Instruction Meaning R-Type Format sa = 10 f = 0 sa = 10 f = 0 s1 \$s1, \$s2, 10 \$s1 = \$s2 <>>10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 0 s1 \$s1, \$s2, 10 \$s1 = \$s2 <>>10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 0 s1 \$s1, \$s2, 10 \$s1 = \$s2 <>>10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 0 s1 \$s1, \$s2, 10 \$s1 = \$s2 <>>10 op = 0 rs = \$s2 rd = \$s1 sa = 0 f = 1 s1 \$s1, \$s2, 10 \$s1 = \$s2 <> \$s3 op = 0x8 rs = \$s2 rd = \$s1 sa = 0 f = 6	subu	\$s1, \$s2, \$s3	\$s1 = \$s2 - \$s3	op =	= 0 rs =	= \$s2	rt =	\$s3 rd	= \$s1	sa = 0	f = 0x23
or \$s1, \$s2, \$s3 \$s1 = \$s2 \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x25 xor \$s1, \$s2, \$s3 \$s1 = \$s2 ^ \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x25 nor \$s1, \$s2, \$s3 \$s1 = \$s2 ^ \$s3 op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x25 Instruction Meaning R-Type Format s1 \$s1, \$s2, 10 \$s1 = \$s2 <<10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 0 f = 0.27 Instruction Meaning R-Type Format s1 \$s1, \$s2, 10 \$s1 = \$s2 <<10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 0 s1 \$s2, \$s3 \$s1 = \$s2 <<10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 0 f = 4 s1 \$s1, \$s2, \$s3 \$s1 = \$s2 <<10 op = 0x8 rs = \$s2 rt = \$s1 imm ¹⁶ = 10 addi \$s1, \$s2, 10 \$s1 = \$s2 + 10 op = 0x4 rs = \$s2 rt = \$s1 imm ¹⁶ = 10											
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	and	\$s1, \$s2, \$s3					<u> </u>				
nor \$s1, \$s2, \$s3 \$s1 = ~(\$s2 \$s3) op = 0 rs = \$s2 rt = \$s3 rd = \$s1 sa = 0 f = 0x27 Instruction Meaning R-Type Format sll \$s1,\$s2,10 \$s1 = \$s2 < <10 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 0 srl \$s1,\$s2,10 \$s1 = \$s2 >>>0 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 0 srl \$s1,\$s2,10 \$s1 = \$s2 >>>0 op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 1 slw \$s1,\$s2,10 \$s1 = \$s2 >>>> op = 0 rs = 0 rt = \$s2 rd = \$s1 sa = 10 f = 3 slw \$s1,\$s2,10 \$s1 = \$s2 >>> op = 0 rs = \$s3 rt = \$s2 rd = \$s1 sa = 0 f = 4 srv \$s1,\$s2,10 \$s1 = \$s2 >>> \$s3 op = 0 rs = \$s2 rt = \$s1 sa = 0 f = 6 srv \$s1,\$s2,10 \$s1 = \$s2 + 10 op = 0x8 rs = \$s2 rt = \$s1 imm ¹⁶ = 10 addi \$s1,\$s2,10 \$s1 = \$s2 + 10 op = 0x6 rs = \$s											
$\begin{array}{ c c c c } \hline \textbf{Meaning} & \textbf{R-Type Format} \\ \hline \textbf{s1} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 2 < 10 & \textbf{op} = 0 & \textbf{rs} = 0 & \textbf{rt} = \textbf{s2}, \textbf{rd} = \textbf{s1} & \textbf{sa} = 10 & \textbf{f} = 0 \\ \textbf{srl} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 2 >> 10 & \textbf{op} = 0 & \textbf{rs} = 0 & \textbf{rt} = \textbf{s2}, \textbf{rd} = \textbf{s1} & \textbf{sa} = 10 & \textbf{f} = 2 \\ \textbf{sra} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 2 >> 10 & \textbf{op} = 0 & \textbf{rs} = 0 & \textbf{rt} = \textbf{s2}, \textbf{rd} = \textbf{s1} & \textbf{sa} = 10 & \textbf{f} = 3 \\ \textbf{s1} & \textbf{s1}, \textbf{s2}, \textbf{s2}, \textbf{s3} & \textbf{s1} = \textbf{s2}, 2 < \textbf{s3} & \textbf{op} = 0 & \textbf{rs} = \textbf{s3}, \textbf{rt} = \textbf{s2}, \textbf{rd} = \textbf{s3}, \textbf{sa} = 0 & \textbf{f} = 4 \\ \textbf{s1v} & \textbf{s1}, \textbf{s2}, \textbf{s3} & \textbf{s1} = \textbf{s2}, 2 >> \textbf{s3} & \textbf{op} = 0 & \textbf{rs} = \textbf{s3}, \textbf{rt} = \textbf{s2}, \textbf{rd} = \textbf{s3}, \textbf{sa} = 0 & \textbf{f} = 6 \\ \textbf{srav} & \textbf{s1}, \textbf{s2}, \textbf{s3}, \textbf{s1} = \textbf{s2}, 2 >> \textbf{s3} & \textbf{op} = 0 & \textbf{rs} = \textbf{s3}, \textbf{rt} = \textbf{s2}, \textbf{rd} = \textbf{s3}, \textbf{sa} = 0 & \textbf{f} = 7 \\ \hline \textbf{nstruction} & \textbf{Meaning} & \textbf{I-Type Format} \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0x8 & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s3}, \textbf{s1} & \textbf{sa} = 0 & \textbf{f} = 7 \\ \hline \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0x8 & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s3}, \textbf{s1} & \textbf{mm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0xc & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s1} & \textbf{imm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0xc & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s1} & \textbf{imm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0xc & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s1} & \textbf{imm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0xc & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s1} & \textbf{imm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0xc & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s1} & \textbf{imm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0xc & \textbf{rs} = \textbf{s2}, \textbf{rt} = \textbf{s1} & \textbf{imm}^{16} = 10 \\ \textbf{addi} & \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, 10 & \textbf{op} = 0 \\ \textbf{s1} = \textbf{s1}, \textbf{s2}, 10 & \textbf{s1} = \textbf{s2}, \textbf{s1} & \textbf{s1} & \textbf{s1} = \textbf{s1} & \textbf{s1} \\ \textbf{s1} \textbf{s1} \textbf{s2}, \textbf{s2}, \textbf{s1} & \textbf{s2} & \textbf{s1} & \textbf{s2} & \textbf{s1}$				<u> </u>	_			_		-	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	nor	\$s1, \$s2, \$s3	\$s1 = ~(\$s2 \$s3)	op =	= 0 rs =	= \$s2	rt =	\$s3 ro	d = \$s1	sa = 0	f = 0x27
$\begin{array}{c c c c c c c c c c c c c c c c c c c $							_				
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				<u> </u>			-	-			
$ \frac{\text{slv} \$s1,\$s2,\$s3}{\text{srs}1,\$s2,\$s3} \$s1 = \$s2 << \$s3}{\text{op} = 0} \hspace{0.5cm} \text{rs} = \$s3} \hspace{0.5cm} t = \$s2 \hspace{0.5cm} $				<u> </u>							
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				<u> </u>				-	-		
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$				<u> </u>							
Instruction Meaning ss1 = \$s2 + 10 Imple op = 0x8 rs = \$s2 rt = \$s1 imm16 = 10 addiu \$s1, \$s2, 10 \$s1 = \$s2 + 10 op = 0x9 rs = \$s2 rt = \$s1 imm16 = 10 andiu \$s1, \$s2, 10 \$s1 = \$s2 + 10 op = 0x9 rs = \$s2 rt = \$s1 imm16 = 10 andi \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0x0 rs = \$s2 rt = \$s1 imm16 = 10 ori \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0xd rs = \$s2 rt = \$s1 imm16 = 10 ori \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0xd rs = \$s2 rt = \$s1 imm16 = 10 xori \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0xe rs = \$s2 rt = \$s1 imm16 = 10 lui \$s1, 10 \$s1 = 10 <<				<u> </u>			-				
addi\$s1, \$s2, 10\$s1 = \$s2 + 10op = 0x8rs = \$s2rt = \$s1imm16 = 10addiu\$s1, \$s2, 10\$s1 = \$s2 + 10op = 0x9rs = \$s2rt = \$s1imm16 = 10andi\$s1, \$s2, 10\$s1 = \$s2 & 10op = 0xcrs = \$s2rt = \$s1imm16 = 10ori\$s1, \$s2, 10\$s1 = \$s2 & 10op = 0xdrs = \$s2rt = \$s1imm16 = 10ori\$s1, \$s2, 10\$s1 = \$s2 & 10op = 0xdrs = \$s2rt = \$s1imm16 = 10xori\$s1, \$s2, 10\$s1 = \$s2 ^ 10op = 0xers = \$s2rt = \$s1imm16 = 10lui\$s1, 10\$s1 = \$s2 ^ 10op = 0xers = \$s2rt = \$s1imm16 = 10lui\$s1, 10\$s1 = \$s2 ^ 10op = 0xers = \$s2rt = \$s1imm16 = 10lui\$s1, 10\$s1 = \$s2 ^ 10op = 0xers = \$s2rt = \$s1imm16 = 10lui\$s1, 10\$s1 = 10 <<	srav	\$\$1,\$\$2,\$\$3	\$\$1 = \$\$2 >> \$\$3	op	= 0 rs	= \$S:	s π =	\$s2 ro	= \$S1	sa = 0	f = 7
addiu \$s1, \$s2, 10 \$s1 = \$s2 + 10 op = 0x9 rs = \$s2 rt = \$s1 imm ¹⁶ = 10 andi \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0xc rs = \$s2 rt = \$s1 imm ¹⁶ = 10 ori \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0xc rs = \$s2 rt = \$s1 imm ¹⁶ = 10 xori \$s1, \$s2, 10 \$s1 = \$s2 ^ 10 op = 0xc rs = \$s2 rt = \$s1 imm ¹⁶ = 10 lui \$s1, 10 \$s1 = \$s2 ^ 10 op = 0xc rs = \$s2 rt = \$s1 imm ¹⁶ = 10 lui \$s1, 10 \$s1 = 10 <<< 16	Inst	ruction									
andi \$s1, \$s2, 10 \$s1 = \$s2 & 10 op = 0xc rs = \$s2 rt = \$s1 imm16 = 10 ori \$s1, \$s2, 10 \$s1 = \$s2 10 op = 0xd rs = \$s2 rt = \$s1 imm16 = 10 xori \$s1, \$s2, 10 \$s1 = \$s2 ^ 10 op = 0xd rs = \$s2 rt = \$s1 imm16 = 10 lui \$s1, \$s2, 10 \$s1 = \$s2 ^ 10 op = 0xf 0 rt = \$s1 imm16 = 10 lui \$s1, 10 \$s1 = \$10 <<< 16 op = 0xf 0 rt = \$s1 imm16 = 10 lui \$s1, 10 \$s1 = 10 <<< 16				<u> </u>	= 0x8	rs =	\$s2	rt = \$			
ori \$s1, \$s2, 10 \$s1 = \$s2 10 op = 0xd rs = \$s2 rt = \$s1 imm ¹⁶ = 10 xori \$s1, \$s2, 10 \$s1 = \$s2 ^ 10 op = 0xe rs = \$s2 rt = \$s1 imm ¹⁶ = 10 lui \$s1, 10 \$s1 = 10 << 16	odd						* *			. 40	
xori \$s1, \$s2, 10 \$s1 = \$s2 ^ 10 op = 0xe rs = \$s2 rt = \$s1 imm ¹⁶ = 10 lui \$s1, 10 \$s1 = 10 << 16 op = 0xf 0 rt = \$s1 imm ¹⁶ = 10 Instruction Meaning Format j label jump to label op ⁶ = 2 imm ¹⁶ beq rs, rt, label branch if (rs == rt) op ⁶ = 4 rs ⁵ rt ⁵ imm ¹⁶ bne rs, rt, label branch if (rs == rt) op ⁶ = 5 rs ⁵ rt ⁵ imm ¹⁶ blez rs, label branch if (rs <=0) op ⁶ = 6 rs ⁵ 0 imm ¹⁶ bgtz rs, label branch if (rs <0) op ⁶ = 1 rs ⁵ 0 imm ¹⁶ bltz rs, label branch if (rs <0) op ⁶ = 1 rs ⁵ 0 imm ¹⁶ bgez rs, label branch if (rs >=0) op ⁶ = 1 rs ⁵ 0 imm ¹⁶ bgez rs, label branch if (rs >=0) op ⁶ = 0 rs ⁵ rt ⁵ 0 ox2 slt rd, rs, rt rd=(rs <rt?1:0)< th=""> op⁶ = 0<td></td><td></td><td></td><td><u> </u></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></rt?1:0)<>				<u> </u>							
Iui $\$s1, 10$ $\$s1 = 10 << 16$ $op = 0xf$ 0 $rt = \$s1$ $imm^{16} = 10$ InstructionMeaning $op^6 = 2$ Formatjlabeljump to label $op^6 = 2$ imm^{26} beqrs, rt, labelbranch if (rs == rt) $op^6 = 4$ rs^5 rt^5 imm^{16} bners, rt, labelbranch if (rs != rt) $op^6 = 5$ rs^5 rt^5 imm^{16} blezrs, labelbranch if (rs <= 0)	andi	\$s1, \$s2, 10	\$s1 = \$s2 & 10	op	= 0xc	rs =	\$s2	rt = \$	s1	imm ¹⁶	= 10
InstructionMeaningFormatjlabeljump to label $op^6 = 2$ imm^{26} beqrs, rt, labelbranch if (rs == rt) $op^6 = 4$ rs^5 rt^5 imm^{16} bners, rt, labelbranch if (rs != rt) $op^6 = 5$ rs^5 rt^5 imm^{16} blezrs, labelbranch if (rs <= 0)	andi ori	\$s1, \$s2, 10 \$s1, \$s2, 10	\$s1 = \$s2 & 10 \$s1 = \$s2 10	op op	= 0xc = 0xd	rs = rs =	\$s2 \$s2	rt = \$ rt = \$	s1 s1	imm ¹⁶ imm ¹⁶	= 10 = 10
jlabeljump to label $op^6 = 2$ imm^{26} beqrs, rt, labelbranch if (rs == rt) $op^6 = 4$ rs^5 rt^5 imm^{16} bners, rt, labelbranch if (rs != rt) $op^6 = 5$ rs^5 rt^5 imm^{16} blezrs, labelbranch if (rs<=0) $op^6 = 6$ rs^5 0 imm^{16} bgtzrs, labelbranch if (rs > 0) $op^6 = 7$ rs^5 0 imm^{16} bgtzrs, labelbranch if (rs < 0) $op^6 = 1$ rs^5 0 imm^{16} bgtzrs, labelbranch if (rs >=0) $op^6 = 1$ rs^5 1 imm^{16} bgzrs, labelbranch if (rs>=0) $op^6 = 1$ rs^5 1 imm^{16} bgzrs, labelbranch if (rs>=0) $op^6 = 1$ rs^5 1 imm^{16} bgzrs, labelbranch if (rs>=0) $op^6 = 1$ rs^5 1 imm^{16} bgzrs, labelbranch if (rs>=0) $op^6 = 0$ rs^5 rt^5 rd^5 0sltrd, rs, rt $rd=(rsop^6 = 0rs^5rt^5rd^500x2aslturd, rs, rtrd=(rsop^6 = 0rs^5rt^5ind^500x2bsltirt, rs, imm^{16}rt=(rs0xars^5rt^5ind^500x2b$	andi ori xori	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10	op op op	= 0xc = 0xd = 0xe	rs = rs = rs =	\$s2 \$s2 \$s2	rt = \$ rt = \$ rt = \$	s1 s1 s1	imm ¹⁶ imm ¹⁶ imm ¹⁶	= 10 = 10 = 10
beq rs, rt, label branch if (rs == rt) $op^6 = 4$ rs^5 rt^5 imm^{16} bne rs, rt, label branch if (rs != rt) $op^6 = 5$ rs^5 rt^5 imm^{16} blez rs, label branch if (rs <= 0)	andi ori xori lui	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	op op op	= 0xc = 0xd = 0xe	rs = rs = rs =	\$s2 \$s2 \$s2	rt = \$ rt = \$ rt = \$ rt = \$	s1 s1 s1 s1	imm ¹⁶ imm ¹⁶ imm ¹⁶	= 10 = 10 = 10
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	andi ori xori lui Inst	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16 Meaning	op op op	= 0xc = 0xd = 0xe = 0xf	rs = rs = rs = (\$s2 \$s2 \$s2	rt = \$ rt = \$ rt = \$ rt = \$	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶	= 10 = 10 = 10
bgtzrs, labelbranch if (rs > 0)op6 = 7rs50imm16bltzrs, labelbranch if (rs < 0)	andi ori xori lui Inst	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label	<pre>\$</pre>	op op op op	= 0xc = 0xd = 0xe = 0xf op ⁶ =	rs = rs = (0 2	\$s2 \$s2 \$s2	rt = \$ rt = \$ rt = \$ rt = \$ For	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶	= 10 = 10 = 10 = 10
bltzrs, labelbranch if (rs < 0)op6 = 1rs50imm16bgezrs, labelbranch if (rs>=0)op6 = 1rs51imm16InstructionMeaningFormatsltrd, rs, rtrd=(rs <rt?1:0)< td="">op6 = 0rs5rt5rd500x2aslturd, rs, rtrd=(rs<rt?1:0)< td="">op6 = 0rs5rt5rd500x2bsltirt, rs, imm16rt=(rs<imm?1:0)< td="">0xars5rt5imm16</imm?1:0)<></rt?1:0)<></rt?1:0)<>	andi ori xori lui Inst j beq	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	op op op op rt)	= 0xc = 0xd = 0xe = 0xf op ⁶ =	rs = rs = () 2 4	\$s2 \$s2) r s ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶	= 10 = 10 = 10 = 10
bgez rs, labelbranch if (rs>=0)op6 = 1rs51imm16InstructionMeaningFormatslt rd, rs, rtrd=(rs <rt?1:0)< td="">op6 = 0rs5rt5rd500x2asltu rd, rs, rtrd=(rs<rt?1:0)< td="">op6 = 0rs5rt5rd500x2bsltu rd, rs, rtrd=(rs<inm?1:0)< td="">0xars5rt5imm16</inm?1:0)<></rt?1:0)<></rt?1:0)<>	andi ori xori lui Inst j beq bne	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label	<pre>\$</pre>	op op op rt)	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ =	rs = rs = () 2 4 5	\$s2 \$s2 \$s2) rs ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For rt ⁵ rt ⁵	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ 26 imm¹⁰	= 10 = 10 = 10 = 10
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	andi ori xori lui Inst j beq bne blez	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, rt, label rs, rt, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	rt)	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ =	rs = rs = (0 2 4 5 6	\$s2 \$s2) rs ⁵ rs ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For rt ⁵ rt ⁵ 0	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ ²⁶ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10
slt rd, rs, rt rd=(rs <rt?1:0)< th=""> op⁶ = 0 rs⁵ rt⁵ rd⁵ 0 0x2a sltu rd, rs, rt rd=(rs<rt?1:0)< td=""> op⁶ = 0 rs⁵ rt⁵ rd⁵ 0 0x2b slti rt, rs, imm¹⁶ rt=(rs<imm?1:0)< td=""> 0xa rs⁵ rt⁵ imm¹⁶</imm?1:0)<></rt?1:0)<></rt?1:0)<>	andi ori xori lui Inst j beq bne blez bgtz	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, rt, label rs, label rs, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	rt)	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ = op ⁶ =	rs = rs = () 2 4 5 6 7	\$s2 \$s2 \$s2) rs ⁵ rs ⁵ rs ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For rt ⁵ rt ⁵ 0 0	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ ²⁶ imm ¹⁰ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10
sltu rd, rs, rt rd=(rs <rt?1:0)< th=""> op⁶ = 0 rs⁵ rt⁵ rd⁵ 0 0x2b slti rt, rs, imm¹⁶ rt=(rs<imm?1:0)< td=""> 0xa rs⁵ rt⁵ imm¹⁶</imm?1:0)<></rt?1:0)<>	andi ori xori lui j beq blez blez bltz	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, rt, label rs, label rs, label rs, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	rt)))	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ = op ⁶ =	rs = rs = () 2 4 5 6 7 1	\$s2 \$s2 \$s2 rs ⁵ rs ⁵ rs ⁵ rs ⁵	rt = \$2 rt = \$2 rt = \$2 rt = \$2 For rt ⁵ rt ⁵ 0 0 0	s1 s1 s1 s1 s1 mat	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁰ 26 imm ¹⁰ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10 = 10 = 10
slti rt, rs, imm ¹⁶ rt=(rs <imm?1:0) 0xa="" rs<sup="">5 rt⁵ imm¹⁶</imm?1:0)>	andi ori xori lui j beq blez blez bltz bgtz bltz	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, rt, label rs, label rs, label rs, label z rs, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	rt)))	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ = op ⁶ =	rs = rs = () 2 4 5 6 7 1	\$s2 \$s2 \$s2 rs ⁵ rs ⁵ rs ⁵ rs ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For rt ⁵ 0 0 0 1	s1 s1 s1 mat imm ²	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁰ 26 imm ¹⁰ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10 = 10 = 10
	andi ori xori lui Inst beq blez blez blez bltz bltz	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, label rs, label rs, label rs, label rs, label rs, label rs, label rs, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	rt)))))	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ = op ⁶ = op ⁶ = op ⁶ =	rs = rs = () 2 4 5 6 7 1 1	\$s2 \$s2 \$s2 rs ⁵ rs ⁵ rs ⁵ rs ⁵ rs ⁵	rt = \$2 rt = \$2 rt = \$2 rt = \$2 For rt ⁵ rt ⁵ 0 0 0 0 1 For	s1 s1 s1 mat imm	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ 26 imm ¹⁰ imm ¹⁰ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10
sltiu rt. rs. imm ¹⁶ rt=(rs <imm?1:0) 0xb="" rs<sup="">5 rt⁵ imm¹⁶</imm?1:0)>	andi ori xori lui j beq blez blez bltz bltz bltz slt	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, label rs, label rs, label rs, label rs, label rs, label rs, label rs, rt, rt, label	\$s1 = \$s2 & 10 \$s1 = \$s2 10 \$s1 = \$s2 ^ 10 \$s1 = \$s2 ^ 10 \$s1 = 10 << 16	op op op rt) rt)))))	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ = op ⁶ = op ⁶ =	rs = rs = () 2 4 5 6 7 1 1 1 1	\$s2 \$s2 \$s2 rs ⁵ rs ⁵ rs ⁵ rs ⁵ rs ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For rt ⁵ rt ⁵ 0 0 0 1 For rt ⁵	s1 s1 s1 mat imm imm mat rd ⁵	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ 26 imm ¹⁰ imm ¹⁰ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10
	andi ori xori lui j beq blez bgtz bltz bgtz bltz slt sltu	\$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, \$s2, 10 \$s1, 10 ruction label rs, rt, label rs, rt, label rs, label rs, label rs, label rs, label rs, label rs, label rs, label rs, rt, rt rd, rs, rt	\$s1 = \$s2 & 10 \$s1 = \$s2 10 <<< 16	op op op rt) rt)))))	= 0xc = 0xd = 0xe = 0xf op ⁶ = op ⁶ = op ⁶ = op ⁶ = op ⁶ = op ⁶ =	rs = rs = () 2 4 5 6 7 1 1 1 1 1 0 0	\$s2 \$s2 \$s2 rs ⁵ rs ⁵ rs ⁵ rs ⁵ rs ⁵ rs ⁵	rt = \$ rt = \$ rt = \$ rt = \$ For rt ⁵ rt ⁵ 0 0 0 1 For rt ⁵ rt ⁵	s1 s1 s1 mat imm imm mat rd ⁵	imm ¹⁶ imm ¹⁶ imm ¹⁶ imm ¹⁶ 26 imm ¹⁰ imm ¹⁰ imm ¹⁰ imm ¹⁰ imm ¹⁰	= 10 = 10 = 10 = 10

Instruction Meaning			I-Type Format					
lb rt, imm ¹⁶ (rs)	rt = MEM[rs+imn	n ¹⁶] 0x2	0 rs	⁵ rt	5	imm ¹⁶		
Ih rt, imm ¹⁶ (rs)	rt = MEM[rs+imn	n ¹⁶] 0x2	1 rs	⁵ rt	5	imn	n ¹⁶	
lw rt, imm ¹⁶ (rs)	rt = MEM[rs+imn	n ¹⁶] 0x2	3 rs	⁵ rt				
Ibu rt, imm16(rs)	u rt, imm ¹⁶ (rs) rt = MEM[rs+imm]		4 rs	⁵ rt	5	imm ¹⁶		
Ihu rt, imm ¹⁶ (rs) rt = MEM[rs+imm		n ¹⁶] 0x2	5 rs	⁵ rt	rt ⁵ imm ¹⁶		n ¹⁶	
sb rt, imm ¹⁶ (rs)	t, imm ¹⁶ (rs) MEM[rs+imm ¹⁶] =		8 rs	⁵ r	t ⁵ imm		n ¹⁶	
sh rt, imm16(rs)	MEM[rs+imm ¹⁶]	= rt 0x2	9 rs	⁵ rt	rt⁵		imm ¹⁶	
sw rt, imm ¹⁶ (rs)	MEM[rs+imm ¹⁶]	= rt 0x2	b rs	⁵ rt	5	imm ¹⁶		
Instruction	Meaning		Format					
jal label S	\$31=PC+4, jump	op ⁶ = 3	p ⁶ = 3 imm ²⁶					
jr Rs	PC = Rs	op ⁶ = 0	rs ⁵	0	0	0	8	
jalr Rd, Rs R	d=PC+4, PC=Rs	op ⁶ = 0	rs ⁵	0	rd ⁵	0	9	
Instruction	Meaning		Format					
mult Rs, Rt	Hi, Lo = <u>Rs</u> × <u>Rt</u>	op ⁶ = 0	Rs⁵	Rt⁵	0	0	0x18	
multu Rs, Rt	Hi, Lo = <u>Rs</u> × <u>Rt</u>	op ⁶ = 0	Rs⁵	Rt⁵	0	0	0x19	
mul Rd, Rs, Rt	Rd = <u>Rs</u> × <u>Rt</u>	0x1c	Rs⁵	Rt⁵	Rd⁵	0	0x02	
div Rs, Rt	Hi, Lo = Rs / Rt	op ⁶ = 0	Rs⁵	Rt⁵	0	0	0x1a	
divu Rs, Rt	Hi, Lo = Rs / Rt	op ⁶ = 0	Rs⁵	Rt⁵	0	0	0x1b	
mfhi Rd	Rd = Hi	op ⁶ = 0	0	0	Rd⁵	0	0x10	
mflo Rd	Rd = Lo	op ⁶ = 0	0	0	Rd⁵	0	0x12	