***King Fahd University of Petroleum and Minerals***

***College of Computer Science and Engineering***

***Computer Engineering Department***

**ICS 233: COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE**

**Term 142 (Spring 2014-2015)**

**Major Exam 1**

**Saturday February 28, 2015**

**Time: 120 minutes, Total Pages: 9**

**Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_\_**

**Notes:**

* Do not open the exam book until instructed
* Answer all questions
* All steps must be shown
* Any assumptions made must be clearly stated

|  |  |  |
| --- | --- | --- |
| **Question** | **Max Points** | **Score** |
| **Q1** | **25** |  |
| **Q2** | **15** |  |
| **Q3** | **20** |  |
| **Total** | **60** |  |

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# **[25 Points]**

# **(Q1)** Fill in the blank in each of the following questions:

## Assuming 8-bit 2`s complement representation, the hexadecimal number EA is equal to the decimal number \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Two advantages of programming in assembly language are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Assuming that variable Array is defined as shown below:

Array: .byte 1, 2, 3, 4, -1, -2, -3, -4

After executing the following sequence of instructions, the content of the three registers is $t1=\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, $t2=\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, and $t3=\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

la $t0, Array

lb $t1, 4($t0)

lhu $t2, 4($t0)

lw $t3, 4($t0)

## Given a magnetic disk with the following properties:

* Rotation speed = 7200 RPM (rotations per minute)
* Average seek = 8 ms, Sector = 512 bytes, Track = 200 sectors

The average time to access a block of 100 consecutive sectors is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ms.

## Assuming the following data segment, and assuming that the first variable X is given the address **0x10010000**, then the addresses for variables Y and Z will be \_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_.

## .data

## X: .byte 1, 2, 3

## Y: .half 4, 5, 6

## Z: .word 7, 8, 9

## Assume that the instruction j NEXT is at address 0x00400010 in the text segment, and the label NEXT is at address 0x00400fec. Then, the address stored in the assembled instruction for the label NEXT is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Assume that the instruction bne $t0, $t1, NEXT is at address 0x00400010 in the text segment, and the label NEXT is at address 0x00400fec. Then, the address stored in the assembled instruction for the label NEXT is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## The pseudo instruction bge $s2, 5, Next is implemented by the following minimum MIPS instructions:

## The pseudo instruction *ori $t0, 0x12345678* is implemented by the following minimum MIPS instructions:

## After executing the instruction addu $t0, $s1, $s2, the following MIPS instruction can be used to store the carry out of addition in register $t1:

## To multiply the **signed** content of register $t0 by 62.5 without using multiplications and division instructions, we use the following MIPS instructions:

## The content of register **$s1** after executing the following code is \_\_\_\_\_\_\_\_\_\_.

li $s0, 0x5a

li $s1, 0

Next:

andi $t0, $s0, 1

add $s1, $s1, $t0

srl $s0, $s0, 1

bne $s0, $0, Next

**[15 Points]**

# **(Q2) Answer the following questions.**

## For what reasons there is a bandwidth mismatch between the speed of processor and the speed of main-memory. How this mismatch problem can be alleviated.

## Since year 2000, the clock frequency of Intel IA32 processors was growing at a rate of approximately 54% per year. In 2000, the reference clock rate was 1.25 GHz. What was the expected clock frequency of IA32 processors in year 2005.

## Consider a binary number A=[a31,….., a0]. Express A as a weighted sum of its components (ai) and their corresponding power of 2 assuming A is (1) unsinged, and (2) signed (2’scomplement). Determine the least and largest values for each of the above two cases.

## Evaluate the decimal value corresponding to the 32-bit signed 2's complement binary number:

1101 0000 0111 1100 1111 1111 1100 0000

## Translate to MIPS assembly the following statement A[15] = A[10] + A[5]+ 5. Assume register $s0 is used to store the base address of array A[], which is an array of words.

**[20 Points]**

# **(Q3)** Write separate MIPS assembly code fragments with **minimum** instructions to implement each of the given requirements.

## Given an array of integers (i.e. words), Array, with its base address stored in register $a0 and its size stored in register $a1, write a MIPS assembly program to store the smallest integer in Array into register $v0.

## Suppose $s1 originally contains 0x12abcd34. Write a MIPS assembly program to extract the 2nd to 5th hexadecimal digits from $s1 and place the extracted data in the upper part of register $s2 and the lower part is filled with zeros.

## Write the most optimized MIPS assembly program to implement the following compound expression:

if ( [($s1 > 0) && ($s2 < 0)] || ($s3 > 0) ) {$s4++;}

## Write the most optimized MIPS assembly program for the following WHILE statement:

## 

i = 0;

WHILE (a[i]+b[i] **<=** k) i = i+1;

Assume $s0 and $s1 are used to store the base addresses of arrays a[] and b[], respectively. $s2 and $s3 are used to store the index i and the value k, respectively. Assume that a[] and b[] are arrays of words.

**MIPS Instructions:**













