KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

ICS 233 Computer Architecture & Assembly Language
Term 081 Lecture Breakdown

	Date	Topics	Ref.
1	S 11/10	Syllabus introduction.	
2	M 13/10	Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages, Why Learn Assembly Language?	Chapter 1: Computer Abstractions and Technology
3	W 15/10	Assembly vs. High-Level Languages, Assembly Language Programming Tools, Assemble and Link Process, Components of a Computer System, Input Devices, Output Devices, Memory, Address Space. Address, Data, and Control Bus, Memory Devices: RAM, DRAM, SRAM, ROM, Magnetic Disk Storage, Processor-Memory Performance Gap.	Chapter 1: Computer Abstractions and Technology
4	S 18/10	Memory Hierarchy, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. Manufacturing Process.	Chapter 1: Computer Abstractions and Technology
5	M 20/10	Effect of Die Size on Yield, Technology Improvements, Programmer's View of a Computer System. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions. Integer Storage Sizes.	Chapter 1: Computer Abstractions and Technology & Chapter 3: Arithmetic for Computers (3.1-3.3)
6	W 22/10	Binary and Hexadecimal Addition, Signed Integers and 2's Complement Notation, Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction, Ranges of Signed Integers.	Chapter 3: Arithmetic for Computers (3.1-3.3) & Chapter 3: Number Systems (Britton Book)
7	S 25/10	Carry and Overflow. **(Quiz#1)**.	Chapter 3: Arithmetic for Computers (3.1-3.3) & Chapter 3: Number Systems (Britton Book)
8	M 27/10	No Class.	
9	W 29/10	Character Storage, ASCII Code. Instruction Set Architecture (ISA). Overview of the MIPS Processor, MIPS, General-Purpose Registers,	Chapter 2: Instructions: Language of the

		MIPS Registers, Conventions, Instruction Formats.	Computer (2.1-2.5) & Chapter 1: The MIPS Architecture (Britton Book)
10	S 1/11	Instruction Categories. R-Type Arithmetic, Logical, and Shift Instructions, Integer Add /Subtract Instructions. Logical Bitwise Instructions: AND, OR, XOR, NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of shift instructions in performing multiplication and division.	Chapter 2: Instructions: Language of the Computer (2.1-2.5) & Chapter 1: The MIPS Architecture (Britton Book)
11	M 3/11	Use of shift instructions in performing multiplication and division. I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. **(Quiz#2)**	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
12	W 5/11	J-Type Format, Conditional Branch Instructions, Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement, Compound Expression with AND.	Chapter 2: Instructions: Language of the Computer (2.6) & Chapter 2: Algorithm Development in Pseudo code & Appendix A (Britton Book)
13	S 8/11	Compound Expression with OR, Signed & Unsigned Comparison. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword, Translating a WHILE Loop. Using Pointers to Traverse Arrays.	Chapter 2: Instructions: Language of the Computer (2.6, 2.8, 2.9) Chapter 2: Algorithm Development in Pseudocode (Britton Book)
14	M 10/11	Copying a String, Summing an Integer Array, Addressing Modes, Branch / Jump Addressing Jump and Branch Limits, PC-Relative Addressing.	Chapter 2: Instructions: Language of the Computer (2.6, 2.8, 2.9) Chapter 2: Algorithm Development in Pseudocode (Britton Book)
	T 11/11	**Midterm Warning**	
15	W 12/11	PC-Relative Addressing. Summary of RISC Design, Assembly Language Statements, Instructions, Comments, Program Template, .DATA, .TEXT, & .GLOBL Directives, Data	Chapter 2: Instructions: Language of the Computer (2.9)

		Definition Statement, Data Directives: .Byte, .Half, .Word, .Float, .double, String Directives: .Ascii, .Aciiz, .Space, Examples of Data Definitions, Memory Alignment, Byte Ordering, Big & Little Endians.	Appendix A.9-A.10 & Appendix A (Britton Book)
	Th 13/11	**Major Exam I**	
16	S 15/11	System Calls, Reading and Printing an Integer, Reading and Printing a String, Reading and Printing a Character, Sum of Three Integers Program. Case Conversion Program.	Appendix A.9-A.10 & Appendix A (Britton Book)
17	M 17/11	Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. Parameter Passing.	Chapter 2: Instructions: Language of the Computer (2.7)
	T 18/11	**Last day dropping with W**	
18	W 19/11	Parameter Passing, Stack Frame, Preserving Registers, Selection Sort Procedure.	Chapter 2: Instructions: Language of the Computer (2.7)
19	S 22/11	Recursive Procedures: factorial. Unsigned Multiplication, Unsigned Multiplication Hardware.	Chapter 2: Instructions: Language of the Computer (2.7) & Chapter 3: Arithmetic for Computers (3.4)
20	M 24/11	Unsigned Multiplication Hardware, Signed Multiplication, Signed Multiplication Hardware. Unsigned Division.	Chapter 3: Arithmetic for Computers (3.4 & 3.5)
21	W 26/11	Division Algorithm & Hardware **(Quiz#3).**	Chapter 3: Arithmetic for Computers (3.5)
22	S 29/11	Signed Division, Multiplication and Division in MIPS. Integer to String Procedure, Floating-Point Numbers, Floating-Point Representation.	Chapter 3: Arithmetic for Computers (3.5 & 3.6)
23	M 1/12	IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation, Converting FP Decimal to Binary, Largest Normalized Float.	Chapter 3: Arithmetic for Computers (3.6)
		Eid Adha Holiday	
24	M 15/12	Review of IEEE 754 Floating-Point Standard, Largest & Smallest Normalized Float, Zero, Infinity, and NaN, Denormalized Numbers, Floating-Point Comparison, Simple 6-bit Floating Point Example, Floating Point Addition / Subtraction.	Chapter 3: Arithmetic for Computers (3.6)
25	W	Floating Point Addition / Subtraction, Floating	Chapter 3: Arithmetic

	17/12	Point Adder Block Diagram.	for Computers (3.6)
26	Th 18/12	Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit, Round and Sticky bits.	Chapter 3: Arithmetic for Computers (3.6)
27	S 20/12	IEEE 754 Rounding Modes. Illustration of Rounding Modes. **(Quiz#4)**	Chapter 3: Arithmetic for Computers (3.6)
28	M 22/12	Floating Point Subtraction Example, Advantages of IEEE 754 Standard, Floating Point Complexities, MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions, Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle.	Chapter 3: Arithmetic for Computers (3.6)
29	W 24/12	What is Performance? Response Time and Throughput, Definition of Performance, CPU Execution Time , Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation. Factors Impacting Performance.	Chapter 4: Assessing and Understanding Performance (4.1, 4.2)
30	S 27/12	Clock Cycles per Instruction (CPI), Performance Equation, Determining the CPI**. (Quiz#5)**	Chapter 4: Assessing and Understanding Performance (4.1, 4.2, 4.5)
31	M 29/12	Determining the CPI, MIPS as a Performance Measure. Drawbacks of MIPS, Amdahl's Law.	Chapter 4: Assessing and Understanding Performance (4.3-4.6)
	T 30/12	**Last day dropping all courses with W**	
32	W 31/12	Amdahl's Law, Benchmarks, The SPEC CPU2000 Benchmarks, SPEC 2000 Ratings (Pentium III & 4), Performance and Power. Single Cycle Processor Design: Designing a Processor: Step-by-Step.	Chapter 4: Assessing and Understanding Performance (4.3-4.6) Chapter 5: The Processor: Datapath & Control (5.1)
33	S 3/1	Designing a Processor: Step-by-Step, Review of MIPS Instruction Formats, Register Transfer Level (RTL), Instructions Executed in Steps, Requirements of the Instruction Set. Components of the Datapath.	Chapter 5: The Processor: Datapath & Control (5.1)
34	M 5/1	Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File.	Chapter 5: The Processor: Datapath & Control (5.2-5.3)
35	W 7/1	Building a Multifunction ALU. Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew,	Chapter 5: The Processor: Datapath & Control (5.2-5.4)

		Instruction Fetching Datapath, Datapath for R-type Instructions	
	Th. 8/1	**Major Exam II**	
36	S 10/1	Datapath for I-type ALU, Instructions, Combining R-type & I-type Datapaths. Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store, Adding Jump and Branch to Datapath.	Chapter 5: The Processor: Datapath & Control (5.2-5.4)
37	M 12/1	Controlling the Execution of Jump & Branch, Main Control. ALU Control, Drawbacks of Single Cycle Processor.	Chapter 5: The Processor: Datapath & Control (5.3-5.4)
38	W 14/1	Multicycle Implementation, Single-cycle vs. Multicycle Performance, Worst Case Timing (Load Instruction), Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining, Synchronous Pipeline, Pipeline Performance, Pipelined Datapath.	Chapter 5: The Processor: Datapath & Control (5.3-5.4) Chapter 6: Enhancing Performance with Pipelining(6.1-6.3)
39	S 17/1	Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance, Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.4)
40	M 19/1	Implementing Forwarding, RAW Hazard Detection, Forwarding Unit. Load Delay, Detecting RAW Hazard after Load, Hazard Detection and Stall Unit.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.4)
	T 20/1	**Dropping all courses with WP/WF**	
41	W 21/1	Compiler Scheduling. WAR Hazard, WAW Hazard, Control Hazards, Reducing the Delay of Branches, Branch Hazard Alternatives, Delayed Branch. Zero-Delayed Branch, Branch Target and Prediction Buffer, Dynamic Branch Prediction, 2-bit Prediction Scheme.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.4, 6.5, 6.6)
42	S 24/1	Random Access Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM, Expanding the Data Bus Width, Increasing Memory Capacity by 2^k, Processor-Memory Performance Gap, The Need for a Memory Hierarchy. Typical Memory Hierarchy, Principle of Locality of Reference.	Chapter 7: Exploiting Memory Hierarchy (7.1) Appendix B.9 (CD)
43	M 26/1	Basics of Caches, Block Placement: Direct Mapped, Fully Associative Cache, Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer.	Chapter 7: Exploiting Memory Hierarchy (7.2, 7.3)
44	W 28/1	Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate,	Chapter 7: Exploiting Memory Hierarchy

		Memory Stall Cycles, CPU Time with Memory Stall Cycles, Designing Memory to Support Caches: Memory Interleaving, Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size.	(7.2, 7.3, 7.5)
45	S 31/1	**NO CLASS.**	