KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

ICS 233 Computer Architecture & Assembly Language
Term 072 Lecture Breakdown

	Date	Topics	Ref.
1	S 16/2	Syllabus introduction. High-Level, Assembly-, and Machine-Languages, Advantages of High-Level Languages, Why Learn Assembly Language?	Chapter 1: Computer Abstractions and Technology
2	M 18/2	Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages, Why Learn Assembly Language? Assembly vs. High-Level Languages, Assembly Language Programming Tools, Assemble and Link Process, Components of a Computer System, Input Devices, Output Devices, Memory, Address Space.	Chapter 1: Computer Abstractions and Technology
3	W 20/2	Memory Devices: RAM, DRAM, SREAM, ROM, Magnetic Disk Storage, Processor-Memory Performance Gap, Memory Hierarchy, Address, Data, and Control Bus, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle.	Chapter 1: Computer Abstractions and Technology
4	S 23/2	Manufacturing Process, Effect of Die Size on Yield, Technology Improvements, Programmer's View of a Computer System. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions.	Chapter 1: Computer Abstractions and Technology & Chapter 3: Arithmetic for Computers (3.1-3.3)
5	M 25/2	Integer Storage Sizes, Binary and Hexadecimal Addition, Signed Integers and 2's Complement Notation, Sign Extension.	Chapter 3: Arithmetic for Computers (3.1-3.3) & Chapter 3: Number Systems (Britton Book)
6	W 27/2	Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction, Ranges of Signed Integers, Carry and Overflow. **(Quiz#1)**	Chapter 3: Arithmetic for Computers (3.1-3.3) & Chapter 3: Number Systems (Britton Book)
7	S 1/3	Carry and Overflow, Character Storage ASCII Code. Parity Bit. Instruction Set Architecture (ISA).	Chapter 2: Instructions: Language of the Computer (2.1-2.5) &

			Chapter 1: The MIPS Architecture (Britton Book)
8	M 3/3	Overview of the MIPS Processor, MIPS, General-Purpose Registers, MIPS Registers, Conventions, Instruction Formats, Instruction Categories. R-Type Arithmetic, Logical, and Shift Instructions, Integer Add /Subtract Instructions.	Chapter 2: Instructions: Language of the Computer (2.1-2.5) & Chapter 1: The MIPS Architecture (Britton Book)
9	W 5/3	Logical Bitwise Instructions: AND, OR, XOR, NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. **(Quiz#2)**	Chapter 2: Instructions: Language of the Computer (2.1-2.5)
10	S 8/3	Use of shift instructions in performing multiplication and division. I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. J-Type Format.	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
11	M 10/3	J-Type Format, Conditional Branch Instructions, Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement, Compound Expression with AND.	Chapter 2: Instructions: Language of the Computer (2.6) & Chapter 2: Algorithm Development in Pseudo code & Appendix A (Britton Book)
12	W 12/3	Compound Expression with OR, Signed & Unsigned Comparison. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword, Translating a WHILE Loop.	Chapter 2: Instructions: Language of the Computer (2.6, 2.8, 2.9) Chapter 2: Algorithm Development in Pseudocode (Britton Book)
13	S 15/3	Translating a WHILE Loop, Using Pointers to Traverse Arrays, Copying a String. **(Quiz#3)**	Chapter 2: Instructions: Language of the Computer (2.6, 2.8, 2.9) Chapter 2: Algorithm Development in Pseudocode (Britton Book)
14	M 17/3	Copying a String, Summing an Integer Array, Addressing Modes, Branch / Jump Addressing PC-Relative Addressing.	Chapter 2: Instructions: Language of the

			Computer (2.6, 2.8, 2.9) Chapter 2: Algorithm Development in Pseudocode (Britton Book)
15	W 19/3	Branch / Jump Addressing Modes, Jump and Branch Limits, PC-Relative Addressing. Summary of RISC Design, Assembly Language Statements, Instructions, Comments, Program Template, .DATA, .TEXT, & .GLOBL Directives, Data Definition Statement, Data Directives: .Byte.	Chapter 2: Instructions: Language of the Computer (2.9) Appendix A.9-A.10 & Appendix A (Britton Book)
16	S 22/3	Data Directives: .Byte, .Half, .Word, .Float, .double, String Directives: .Ascii, .Aciiz, .Space, Examples of Data Definitions, Memory Alignment, Byte Ordering and, Big & Little Endians, System Calls, Reading and Printing an Integer, Reading and Printing a String, Reading and Printing a Character, Sum of Three Integers Program.	Appendix A.9-A.10 & Appendix A (Britton Book)
17	M 24/3	Case Conversion Program, Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR.	Chapter 2: Instructions: Language of the Computer (2.7)
18	W 26/3	Parameter Passing, Stack Frame, Preserving Registers, Selection Sort Procedure.	Chapter 2: Instructions: Language of the Computer (2.7)
	Th 27/3	**Major Exam I**	
19	S 29/3	Recursive Procedures: factorial. Unsigned Multiplication, Unsigned Multiplication Hardware.	Chapter 2: Instructions: Language of the Computer (2.7) & Chapter 3: Arithmetic for Computers (3.4)
20	M 31/3	Unsigned Multiplication Hardware, Signed Multiplication, Signed Multiplication Hardware.	Chapter 3: Arithmetic for Computers (3.4)
21	W 2/4	Faster Multiplication Hardware, Carry Save Adders, Unsigned Division , Division Algorithm & Hardware, Signed Division. **(Quiz#4)**	Chapter 3: Arithmetic for Computers (3.5)
22	S 5/4	Faster Multiplication Hardware, Carry Save Adders, Unsigned Division**. (Solution of Major Exam I).**	Chapter 3: Arithmetic for Computers (3.5)
23	M 7/4	Division Algorithm & Hardware, Signed Division, Multiplication and Division in MIPS. Integer to String Procedure, Floating-Point Numbers.	Chapter 3: Arithmetic for Computers (3.5 & 3.6)

24	W 9/4	Floating-Point Representation, IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation, Converting FP Decimal to Binary, Largest & Smallest Normalized Float.	Chapter 3: Arithmetic for Computers (3.6)
		Midterm Break	
25	S 19/4	Review of IEEE 754 Floating-Point Standard, Zero, Infinity, and NaN, Denormalized Numbers, Floating-Point Comparison, Floating Point Addition / Subtraction.	Chapter 3: Arithmetic for Computers (3.6)
26	M 21/4	Simple 6-bit Floating Point Example Floating Point Addition / Subtraction, Floating Point Adder Block Diagram. (**Quiz#5)**	Chapter 3: Arithmetic for Computers (3.6)
27	W 23/4	Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit, Round and Sticky bits. IEEE 754 Rounding Modes.	
28	S 26/4	Illustration of Rounding Modes, Floating Point Subtraction Example, Advantages of IEEE 754 Standard, Floating Point Complexities, MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions, Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle.	Chapter 3: Arithmetic for Computers (3.6)
29	M 28/4	What is Performance?, Response Time and Throughput, Definition of Performance, CPU Execution Time , Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation.	Chapter 4: Assessing and Understanding Performance (4.1)
30	W 30/4	Factors Impacting Performance. (**Quiz#6)**	Chapter 4: Assessing and Understanding Performance (4.1, 4.2)
31	S 3/5	Clock Cycles per Instruction (CPI), Performance Equation, Determining the CPI, MIPS as a Performance Measure.	Chapter 4: Assessing and Understanding Performance (4.1, 4.2, 4.5)
32	M 5/5	MIPS as a Performance Measure, Drawbacks of MIPS, Amdahl's Law, Benchmarks, The SPEC CPU2000 Benchmarks, SPEC 2000 Ratings (Pentium III & 4), Performance and Power.	Chapter 4: Assessing and Understanding Performance (4.3-4.6)
33	W 7/5	Performance and Power, Energy Efficiency, Single Cycle Processor Design: Designing a Processor: Step-by-Step, Review of MIPS Instruction Formats, Register Transfer Level (RTL), Instructions Executed in Steps, Requirements of the Instruction Set.	Chapter 4: Assessing and Understanding Performance (4.3-4.6) Chapter 5: The

			Processor: Datapath & Control (5.1)
34	S 10/5	Components of the Datapath, Register Element, MIPS Register File, Tri-State Buffers. **(Quiz#7)**	Chapter 5: The Processor: Datapath & Control (5.2-5.3)
35	M 12/5	Designing the MIPS Register File.	Chapter 5: The Processor: Datapath & Control (5.2-5.3)
36	W 14/5	Building a Multifunction ALU.	Chapter 5: The Processor: Datapath & Control (5.2-5.3)
37	S 17/5	Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew, Instruction Fetching Datapath, Datapath for R-type Instructions, Datapath for I-type ALU, Instructions, Combining R-type & I-type Datapaths. Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store, Adding Jump and Branch to Datapath.	Chapter 5: The Processor: Datapath & Control (5.2-5.4)
	S 17/5	**Major Exam II**	
38	M 19/5	Details of Next PC, Controlling the Execution of Jump & Branch, Main Control.	Chapter 5: The Processor: Datapath & Control (5.3-5.4)
39	W 21/5	ALU Control, Drawbacks of Single Cycle Processor. Multicycle Implementation, Single-cycle vs. Multicycle Performance, Worst Case Timing (Load Instruction), Pipelined Processor Design: Pipelining Example.	Chapter 5: The Processor: Datapath & Control (5.3-5.4) Chapter 6: Enhancing Performance with Pipelining(6.1-6.2
40	S 24/5	Serial execution versus Pipelining, Synchronous Pipeline, Pipeline Performance, Pipelined Datapath.	Chapter 6: Enhancing Performance with Pipelining(6.1-6.3)
41	M 26/5	Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance, Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards, Implementing Forwarding, RAW Hazard Detection, Forwarding Unit.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.4)
42	W 28/5	Load Delay, Detecting RAW Hazard after Load, Hazard Detection and Stall Unit, Compiler Scheduling. WAR Hazard, WAW Hazard, Control Hazards, Reducing the Delay of Branches, Branch Hazard Alternatives, Delayed Branch.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.4, 6.5, 6.6)
43	S 31/5	Zero-Delayed Branch, Branch Target and Prediction Buffer, Dynamic Branch Prediction, 2-bit Prediction Scheme. Random Access	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.6)

		Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM, Expanding the Data Bus Width, Increasing Memory Capacity by 2^k, Processor-Memory Performance Gap, The Need for a Memory Hierarchy. Typical Memory Hierarchy, Principle of Locality of Reference.	Chapter 7: Exploiting Memory Hierarchy (7.1) Appendix B.9 (CD)
44	M 2/6	Basics of Caches, Block Placement: Direct Mapped, Fully Associative Cache, Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer.	Chapter 7: Exploiting Memory Hierarchy (7.2, 7.3)
45	W 4/6	Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles, Designing Memory to Support Caches: Memory Interleaving, Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size.	Chapter 7: Exploiting Memory Hierarchy (7.2, 7.3, 7.5)