KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COLLEGE OF COMPUTER SCIENCES & ENGINEERING

ICS 233 Computer Architecture & Assembly Language
Term 063 Lecture Breakdown

	Date	Topics	Ref.
1	U 1/7	Syllabus introduction. High-Level, Assembly-, and Machine-Languages, Advantages of High-Level Languages, Why Learn Assembly Language?	Chapter 1: Computer Abstractions and Technology
2	M 2/7	Assembly Language Programming Tools, Components of a Computer System, Memory Devices, Magnetic Disk Storage, Memory Hierarchy, Address, Data, and Control Bus	Chapter 1: Computer Abstractions and Technology
3	T 3/7	Processor: datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle, Chip Manufacturing Process, Effect of Die Size on Yield, Technology Improvements, Programmer's View of a Computer System.	Chapter 1: Computer Abstractions and Technology
4	W 4/7	Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions, Integer Storage Sizes, Binary and Hexadecimal Addition, Signed Integers and 2's Complement Notation, Sign Extension	Chapter 3: Arithmetic for Computers (3.1-3.3) & Chapter 3: Number Systems (Britton Book)
5	S 7/7	Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction, Ranges of Signed Integers, Carry and Overflow, Character Storage ASCII Code.	Chapter 3: Arithmetic for Computers (3.1-3.3) & Chapter 3: Number Systems (Britton Book)
6	U 8/7	Parity Bit. Instruction Set Architecture (ISA), Overview of the MIPS Processor, MIPS, General-Purpose Registers, MIPS Registers, Conventions, Instruction Formats, Instruction Categories.	Chapter 2: Instructions: Language of the Computer (2.1-2.5) & Chapter 1: The MIPS Architecture (Britton Book)
7	M 9/7	R-Type Arithmetic, Logical, and Shift Instructions, Integer Add /Subtract Instructions Logical Bitwise Instructions, Shift Instructions. Applications of logical instructions. Use of shift instructions in performing multiplication and division.	Chapter 2: Instructions: Language of the Computer (2.1-2.5)
8	T 10/7	I-Type Format, I-Type ALU Instructions, 32-bit Constants, J-Type Format, Conditional Branch Instructions, Set on Less Than Instructions,	Chapter 2: Instructions: Language of the

		Pseudo-Instructions.	Computer (2.6)
9	S 14/7	Pseudo-Instructions, Jump, Branch, and SLT Instructions, Translating an IF Statement, Compound Expression with AND, Compound Expression with OR, Signed & Unsigned Comparison. **(QUIZ#1)**	Chapter 2: Instructions: Language of the Computer (2.6) & Chapter 2: Algorithm Development in Pseudocode & Appendix A (Britton Book)
10	U 15/7	Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword, Translating a WHILE Loop, Using Pointers to Traverse Arrays, Copying a String, Summing an Integer Array, Addressing Modes, Branch / Jump Addressing Modes.	Chapter 2: Instructions: Language of the Computer (2.6, 2.8, 2.9) Chapter 2: Algorithm Development in Pseudocode (Britton Book)
11	M 16/7	Branch / Jump Addressing Modes, Jump and Branch Limits, Summary of RISC Design, Assembly Language Statements, Instructions, Comments, Program Template, .DATA, .TEXT, & .GLOBL Directives, Data Definition Statement, Data Directives, String Directives.	Chapter 2: Instructions: Language of the Computer (2.9) Appendix A.9-A.10 & Appendix A (Britton Book)
12	T 17/7	String Directives, Examples of Data Definitions, Memory Alignment, Byte Ordering and, Endianness, System Calls, Reading and Printing an Integer, Reading and Printing a String, Reading and Printing a Character, Sum of Three Integers Program, Case, Conversion Program	Appendix A.9-A.10 & Appendix A (Britton Book)
13	U 22/7	Procedures, Call / Return Sequence, Instructions for Procedures, Parameter Passing, Stack Frame, Preserving Registers, Selection Sort Procedure, Recursive Procedures.	Chapter 2: Instructions: Language of the Computer (2.7)
	U 22/7	MAJOR EXAM I	
14	M 23/7	Unsigned Multiplication, Unsigned Multiplication Hardware, Signed Multiplication, Signed Multiplication Hardware, Faster Multiplication Hardware.	Chapter 3: Arithmetic for Computers (3.4)
15	T 24/7	Carry Save Adders, Unsigned Division , Division Algorithm & Hardware, Signed Division, Multiplication and Division in MIPS.	Chapter 3: Arithmetic for Computers (3.5)
16	W 25/7	Integer to String Procedure, Floating-Point Numbers. **(Solution of EXAM I)**	Chapter 3: Arithmetic for Computers (3.6)
17	S 28/7	Floating-Point Representation, IEEE 754 Floating-Point Standard, Normalized Floating	Chapter 3: Arithmetic for Computers (3.6)

		Point Numbers, Biased Exponent Representation, Converting FP Decimal to Binary, Largest & Smallest Normalized Float, Zero, Infinity, and NaN, Denormalized Numbers, Floating-Point Comparison, Floating Point Addition.	
18	U 29/7	Floating Point Addition / Subtraction, Floating Point Adder Block Diagram, Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit.	Chapter 3: Arithmetic for Computers (3.6)
19	M 30/7	Guard Bit, Round and Sticky Bits, IEEE 754 Rounding Modes, MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions, Data Movement Instructions, Convert Instructions, Compare and Branch Instructions. **(QUIZ#2)**	Chapter 3: Arithmetic for Computers (3.6)
20	T 31/7	FP Data Directives, FP Syscall Services Examples: Area of a circle, Matrix Multiplication. What is Performance?, Response Time and Throughput, Definition of Performance, CPU Execution Time , Improving Performance.	Chapter 3: Arithmetic for Computers (3.6) & Chapter 4: Assessing and Understanding Performance (4.1)
21	S 4/8	Clock Cycles per Instruction (CPI), Performance Equation, Determining the CPI, MIPS as a Performance Measure, Drawbacks of MIPS, Amdahl's Law.	Chapter 4: Assessing and Understanding Performance (4.1, 4.2, 4.5)
22	U 5/8	Amdahl's Law, Benchmarks, The SPEC CPU2000 Benchmarks, SPEC 2000 Ratings (Pentium III & 4), Performance and Power, Energy Efficiency, Single Cycle Processor Design: Designing a Processor: Step-by-Step, Review of MIPS Instruction Formats, Register Transfer Level (RTL), Instructions Executed in Steps, Requirements of the Instruction Set.	Chapter 4: Assessing and Understanding Performance (4.3-4.6) Chapter 5: The Processor: Datapath & Control (5.1)
23	M 6/8	Components of the Datapath, Register Element, MIPS Register File, Tri-State Buffers.	Chapter 5: The Processor: Datapath & Control (5.2-5.3)
24	T 7/8	Building a Multifunction ALU, Instruction and Data Memories, Clocking Methodology Determining the Clock Cycle, Clock Skew, Instruction Fetching Datapath, Datapath for R-type Instructions, Datapath for I-type ALU, Instructions, Combining R-type & I-type Datapaths.	Chapter 5: The Processor: Datapath & Control (5.2-5.3)
25	U 12/8	Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store, Adding Jump and Branch to Datapath Details of Next PC, Controlling the Execution of	Chapter 5: The Processor: Datapath & Control (5.3-5.4)

		Jump & Branch, Main Control and ALU Control, Drawbacks of Single Cycle Processor.	
26	M 13/8	Multicycle Implementation, Single-cycle vs. Multicycle Performance, Worst Case Timing (Load Instruction), Pipelined Processor Design: Pipelining Example, Serial execution versus Pipelining, Synchronous Pipeline, Pipeline Performance, Pipelined Datapath, Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance, Pipelined Control.	Chapter 5: The Processor: Datapath & Control (5.4) Chapter 6: Enhancing Performance with Pipelining(6.1-6.3)
	M 13/8	MAJOR EXAM II	
27	T 14/8	Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards, Implementing Forwarding, RAW Hazard Detection, Forwarding Unit, Load Delay, Detecting RAW Hazard after Load, Hazard Detection and Stall Unit, Compiler Scheduling.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.4, 6.5)
28	W 15/8	WAR Hazard, WAW Hazard, Control Hazards, Reducing the Delay of Branches, Branch Hazard Alternatives, Delayed Branch, Zero-Delayed Branch, Branch Target and Prediction Buffer, Dynamic Branch Prediction, 2-bit Prediction Scheme.	Chapter 6: Enhancing Performance with Pipelining(6.1, 6.6)
29	S 18/8	Random Access Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM, Expanding the Data Bus Width, Increasing Memory Capacity by 2^k, Processor-Memory Performance Gap, The Need for a Memory Hierarchy.	Chapter 7: Exploiting Memory Hierarchy (7.1) Appendix B.9 (CD)
30	U 19/8	Typical Memory Hierarchy, Principle of Locality of Reference, Basics of Caches, Block Placement: Direct Mapped, Fully Associative Cache, Set-Associative Cache.	Chapter 7: Exploiting Memory Hierarchy (7.2, 7.3)
31	M 20/8	Set-Associative Cache, Write Policy, Write Miss Policy, Write Buffer, Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles, Designing Memory to Support Caches: Memory Interleaving, Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size.	Chapter 7: Exploiting Memory Hierarchy (7.2, 7.3, 7.5)