

KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

ICS 233 Computer Architecture & Assembly Language

Term 142 Lecture Breakdown

| Lec # | Date | Topics | Ref. |
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| 1 | T 27/1 | Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages, Why Learn Assembly Language? Assembly vs. High-Level Languages, Assembly Language Programming Tools. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 2 | TH 29/1 | Assembly Language Programming Tools, Assemble and Link Process, Components of a Computer System, Memory, Address Space. Address, Data, and Control Bus. Memory Devices: RAM, DRAM, SRAM, ROM. Magnetic Disk Storage, Processor-Memory Performance Gap. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 3 | U 1/2 | Processor-Memory Performance Gap. Memory Hierarchy, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. Technology Improvements. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 4 | T 3/2 | Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions. Integer Storage Sizes. Binary and Hexadecimal Addition. | |
| 5 | TH 5/2 | Signed Integers and 2's Complement Notation, Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction, Ranges of Signed Integers. Carry and Overflow. | |
| 6 | U 8/2 | Character representation, parity bit. Overview of the MIPS, Processor, MIPS, General-Purpose Registers, Conventions, Instruction Formats. Instruction Categories. | Chapter 2: Instructions: Language of the Computer (2.1-2.2) |
| 7 | T 10/2 | Instruction Categories. R-Type Arithmetic, Logical, and Shift Instructions, Integer Add/Subtract Instructions. Logical Bitwise Instructions: AND, OR, XOR, NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of | Chapter 2: Instructions: Language of the Computer (2.1-2.6) |

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| | | shift instructions in performing multiplication and division. (Quiz#1) | |
| 8 | TH 12/2 | Use of shift instructions in performing multiplication and division. I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. J-Type Format. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 9 | U 15/2 | Conditional Branch Instructions, Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement, Compound Expression with AND. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 10 | T 17/2 | Compound Expression with OR, Signed & Unsigned Comparison. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 11 | TH 19/2 | Translating a WHILE Loop. Using Pointers to Traverse Arrays. Copying a String, Summing an Integer Array. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 12 | U 22/2 | Addressing Modes, Branch / Jump Addressing Jump and Branch Limits, PC-Relative Addressing. Summary of RISC Design, Assembly Language Statements, Instructions, Comments, Program Template. Data Definition Statement, Data Directives: .Byte, .Half, .Word, .Float, .double, String Directives: .Ascii, .Asciiz, .Space, Examples of Data Definitions, Memory Alignment. | 2.10 Appendix A.9-A.10 |
| 13 | T 24/2 | Byte Ordering, Big & Little Endians. System Calls, Reading and Printing an Integer, Reading and Printing a String, Reading and Printing a Character. System Calls, Sum of Three Integers Program. (Quiz#2) | Appendix A.9-A.10 |
| 14 | TH 26/2 | Case Conversion Program. File operations. Review for Major Exam 1. | Appendix A.9-A.10 |
| | S 28/2 | Major Exam I | |
| 15 | U 1/3 | Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. Parameter Passing, Stack Frame, Preserving Registers. | Chapter 2: Instructions: Language of the Computer (2.8) |
| 16 | T 3/3 | Parameter Passing, Stack Frame, Preserving Registers. Selection Sort Procedure. | Chapter 2: Instructions: Language of the Computer (2.8) |
| | TH 5/3 | Last Day for Dropping with W | |
| 17 | TH 5/3 | Selection Sort Procedure. Recursive Procedures: factorial. Unsigned Multiplication Hardware, Signed Multiplication. | Chapter 3: Arithmetic for Computers (3.3) |

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| 18 | U 8/3 | Signed Multiplication Hardware. Fast Multiplication, Unsigned Division. Division Algorithm & Hardware. Signed Division, Multiplication and Division in MIPS. | Chapter 3: Arithmetic for Computers (3.3-3.4) |
| 19 | T 10/3 | Integer to String Procedure. Floating-Point Numbers, Floating-Point Representation. IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation. Converting FP Decimal to Binary, Largest & Smallest Normalized Float, Zero, Infinity, and NaN, Denormalized Numbers. Floating-Point Comparison. | Chapter 3: Arithmetic for Computers (3.5) |
| 20 | TH 12/3 | Simple 6-bit Floating Point Example. Floating Point Addition/Subtraction, Floating Point Adder Block Diagram. | Chapter 3: Arithmetic for Computers (3.5) |
| 21 | U 15/3 | Floating Point Addition/Subtraction, Floating Point Adder Block Diagram. Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit, Round and Sticky bits. IEEE 754 Rounding Modes. | Chapter 3: Arithmetic for Computers (3.5) |
| 22 | T 17/3 | IEEE 754 Rounding Modes. MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions. (Quiz#3) | Chapter 3: Arithmetic for Computers (3.5) |
| 23 | TH 19/3 | MIPS Floating-Point Instructions: Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle, matrix multiplication. | Chapter 3: Arithmetic for Computers (3.5) |
| | 20-28/3 | MIDTERM VACATION | |
| 24 | U 29/3 | Single Cycle Processor Design: Designing a Processor: Step-by-Step. Review of MIPS Instruction Formats, Register Transfer Level (RTL). Instructions Executed in Steps, Requirements of the Instruction Set. Components of the Datapath. Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File. | 4.1-4.3 |
| 25 | T 31/3 | Building a Multifunction ALU, Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew. | 4.1-4.3 |
| 26 | TH 3/4 | (Quiz#4) | |
| 27 | S 4/4 | No Class | |
| 28 | U 5/4 | No Class | |
| 29 | T 7/4 | Instruction Fetching Datapath, Datapath for R-type Instructions. Datapath for I-type ALU, Instructions, Combining R-type & I-type Datapaths. Controlling ALU Instructions, Details of the Extender, Controlling the | 4.1-4.3 |

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| | | Execution of Load & Store. Adding Jump and Branch to Datapath. Controlling the Execution of Jump & Branch. | |
| | TH 9/4 | Last Day for Dropping all Courses with W | |
| 30 | TH 9/4 | Main Control. ALU Control. Worst Case Timing (Load Instruction). | 4.1-4.4 |
| 31 | U 12/4 | What is Performance? Factors affecting execution time. Response Time and Throughput, Definition of Performance, CPU Execution Time, Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation. Factors Impacting Performance. | 1.6 |
| 32 | T 14/4 | Determining the CPI. Amdahl's Law. | 1.6 |
| 33 | TH 16/4 | Benchmarks, The SPEC CPU2000 Benchmarks. Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining, Synchronous Pipeline, Pipeline Performance. Pipelined Datapath. | 1,6 & 4.5-4.6 |
| | U 19/4 | Major Exam II | |
| 34 | U 19/4 | Instruction-Time Diagram, Single-Cycle vs. Pipelined Performance, Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards. Implementing Forwarding, RAW Hazard Detection. Forwarding Unit. | 4.6-4.8 |
| 35 | T 21/4 | Load Delay, Detecting RAW Hazard after Load, Hazard Detection and Stall Unit. | 4.8 |
| 36 | TH 23/4 | Compiler Scheduling. WAR Hazard, WAW Hazard. Control Hazards. | 4.8 |
| 37 | U 26/4 | Reducing the Delay of Branches, Branch Hazard Alternatives, Delayed Branch. | 4.8 |
| 38 | T 28/4 | Random Access Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM. | 5.1-5.2 |
| 39 | TH 30/4 | Expanding the Data Bus Width, Increasing Memory Capacity by 2^k . Processor-Memory Performance Gap, The Need for a Memory Hierarchy. Typical Memory Hierarchy. (Quiz#5) | 5.1-5.3 |
| 40 | U 3/5 | Principle of Locality of Reference. Basics of Caches, Block Placement: Direct Mapped. | 5.1-5.3 |
| 41 | T 5/5 | Fully Associative Cache, Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer. | 5.1-5.4 |
| | TH 7/5 | Dropping all Courses with WP/WF | |

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| 42 | TH 7/5 | Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles. Improving Cache Performance: Average Memory Access Time. | 5.1-5.4 |
| 43 | U 10/5 | Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size. | 5.4 |
| 44 | T 12/5 | Zero-Delayed Branch, Branch Target and Prediction Buffer (Quiz#6) | 4.8 |
| 45 | TH 14/5 | Dynamic Branch Prediction, 2-bit Prediction Scheme. Review for the final exam. | 4.8 |