# KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
## *COMPUTER ENGINEERING DEPARTMENT*

## ICS 233 Computer Architecture & Assembly Language

### Term 141 Lecture Breakdown

| Lec # | Date | Topics | Ref. |
|---|---|---|---|
| 1 | U 31/8 | Syllabus introduction. | |
| 2 | T 2/9 | Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages, Why Learn Assembly Language? Assembly vs. High-Level Languages, Assembly Language Programming Tools. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 3 | TH 4/9 | Assembly Language Programming Tools, Assemble and Link Process, Components of a Computer System, Input Devices, Output Devices, Memory, Address Space. Address, Data, and Control Bus. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 4 | U 7/9 | Memory Devices: RAM, DRAM, SRAM, ROM, Magnetic Disk Storage, Processor-Memory Performance Gap. Memory Hierarchy, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 5 | T 9/9 | Fetch-Execute Cycle. Manufacturing Process. Effect of Die Size on Yield. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 6 | TH 11/9 | Technology Improvements, Programmer's View of a Computer System. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions. Integer Storage Sizes. | Chapter 1: Computer Abstractions and Technology 1.1-1.5 |
| 7 | U 14/9 | Binary and Hexadecimal Addition, Signed Integers and 2's Complement Notation, Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction, Ranges of Signed Integers. Carry and Overflow. | |

| | | | |
|---|---|---|---|
| 8 | T 16/9 | Overview of the MIPS, Processor, MIPS, General-Purpose Registers, Conventions, Instruction Formats. **(Quiz#1)** | Chapter 2: Instructions: Language of the Computer (2.1-2.2) |
| 9 | TH 18/9 | Instruction Categories. R-Type Arithmetic, Logical, and Shift Instructions, Integer Add /Subtract Instructions. Logical Bitwise Instructions: AND, OR, XOR, NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of shift instructions in performing multiplication and division. | Chapter 2: Instructions: Language of the Computer (2.1-2.6) |
| 10 | U 21/9 | Use of shift instructions in performing multiplication and division. I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. J-Type Format, Conditional Branch Instructions, Set on Less Than Instructions, Pseudo-Instructions. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| | T 23/9 | National Day - Holiday | |
| 11 | TH 25/9 | Conditional Branch Instructions, Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement, Compound Expression with AND. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| | 26/9 – 11/10 | Id al-Adha Vacation | |
| 12 | U 12/10 | Compound Expression with OR, Signed & Unsigned Comparison. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword, Translating a WHILE Loop. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 13 | T 14/10 | Using Pointers to Traverse Arrays. Copying a String, Summing an Integer Array. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 14 | TH 16/10 | Addressing Modes, Branch / Jump Addressing Jump and Branch Limits, PC-Relative Addressing. Summary of RISC Design, Assembly Language Statements, Instructions, Comments, Program Template. | 2.10 |
| 15 | U 19/10 | Data Definition Statement, Data Directives: .Byte, .Half, .Word, .Float, .double, String Directives: .Ascii, .Aciiz, .Space, Examples of Data Definitions, Memory Alignment, Byte Ordering, Big & Little Endians. System Calls, Reading and Printing an Integer, Reading and Printing a String, Reading and Printing a Character. | Appendix A.9-A.10 |
| 16 | T 21/10 | System Calls, Sum of Three Integers Program. Case Conversion Program. File operations. | Appendix A.9-A.10 |

| | | | |
|---|---|---|---|
| 17 | TH 23/10 | Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. | Chapter 2: Instructions: Language of the Computer (2.8) |
| | TH 23/10 | **Last Day for Dropping with W** | |
| 18 | U 26/10 | **(Quiz#2)** | |
| 19 | T 28/10 | Parameter Passing, Stack Frame, Preserving Registers. | Chapter 2: Instructions: Language of the Computer (2.8) |
| 20 | TH 30/10 | Parameter Passing, Stack Frame, Preserving Registers. | Chapter 2: Instructions: Language of the Computer (2.8) |
| 21 | U 2/11 | Selection Sort Procedure. Recursive Procedures: factorial. **(Quiz#3)** | Chapter 2: Instructions: Language of the Computer (2.8) |
| 22 | T 4/11 | Unsigned Multiplication Hardware, Signed Multiplication, Signed Multiplication Hardware. | Chapter 3: Arithmetic for Computers (3.3) |
| 23 | TH 6/11 | Fast Multiplication, Unsigned Division. Division Algorithm & Hardware. Signed Division, Multiplication and Division in MIPS. Integer to String Procedure. | Chapter 3: Arithmetic for Computers (3.3-3.4) |
| 24 | U 9/11 | Floating-Point Numbers, Floating-Point Representation. IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation, Converting FP Decimal to Binary, Largest & Smallest Normalized Float, Zero, Infinity, and NaN, Denormalized Numbers. | Chapter 3: Arithmetic for Computers (3.5) |
| 25 | T 11/11 | Denormalized Numbers, Floating-Point Comparison, Simple 6-bit Floating Point Example, Floating Point Addition. | Chapter 3: Arithmetic for Computers (3.5) |
| 26 | TH 13/11 | Floating Point Subtraction, Floating Point Adder Block Diagram. Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit, Round and Sticky bits. IEEE 754 Rounding Modes. | Chapter 3: Arithmetic for Computers (3.5) |
| 27 | U 16/11 | Floating Point Addition/Subtraction Example, IEEE 754 Rounding Modes, Advantages of IEEE 754 Standard, Floating Point Complexities. | Chapter 3: Arithmetic for Computers (3.5) |
| 28 | T 18/11 | MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions, Data Movement Instructions, Convert Instructions, | Chapter 3: Arithmetic for Computers (3.5) |

| | | | |
|---|---|---|---|
| | | Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle. **(Quiz#4)** | |
| 29 | TH 20/11 | Matrix Multiplication. What is Performance? Factors affecting execution time. | 1.6 |
| | TH 20/11 | **Last Day for Dropping all Courses with W** | |
| | S 22/11 | **Midterm Exam** | |
| 30 | U 23/11 | Response Time and Throughput, Definition of Performance, CPU Execution Time, Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation. Factors Impacting Performance. Determining the CPI. | 1.6 |
| 31 | T 25/11 | Determining the CPI, MIPS as a Performance Measure. Drawbacks of MIPS, Amdahl's Law. | 1.6 |
| 32 | TH 27/11 | Benchmarks, The SPEC CPU2000 Benchmarks, SPEC 2000 Ratings (Pentium III & 4), Performance and Power. Single Cycle Processor Design: Designing a Processor: Step-by-Step. Review of MIPS Instruction Formats, Register Transfer Level (RTL). | 4.1-4.3 |
| 33 | U 30/11 | Instructions Executed in Steps, Requirements of the Instruction Set. Components of the Datapath. Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File. Building a Multifunction ALU. | 4.1-4.3 |
| 34 | T 2/12 | Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew, Instruction Fetching Datapath, Datapath for R-type Instructions. Datapath for I-type ALU, Instructions, Combining R-type & I-type Datapaths. Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store. | 4.1-4.3 |
| 35 | TH 4/12 | Adding Jump and Branch to Datapath. Controlling the Execution of Jump & Branch **(Quiz#5)** | 4.1-4.3 |
| 36 | U 7/12 | Main Control. ALU Control, Drawbacks of Single Cycle Processor. Multicycle Implementation, Single-cycle vs. Multicycle Performance. | 4.4 |
| 37 | T 9/12 | Worst Case Timing (Load Instruction), Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining, Synchronous Pipeline, Pipeline Performance. | 4.5 |
| 38 | TH 11/12 | Pipelined Datapath. Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance, Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards. | 4.6 |

| | | | |
|---|---|---|---|
| 39 | U 14/12 | Data Hazards. Implementing Forwarding, RAW Hazard Detection, Forwarding Unit. Load Delay. | 4.7 |
| 40 | T 16/12 | Load Delay, Detecting RAW Hazard after Load, Hazard Detection and Stall Unit. Compiler Scheduling. WAR Hazard, WAW Hazard, Control Hazards. | 4.7 & 4.8 |
| 41 | TH 18/12 | Control Hazards, Reducing the Delay of Branches, Branch Hazard Alternatives, Delayed Branch. Zero-Delayed Branch, Branch Target and Prediction Buffer, Dynamic Branch Prediction. | 4.8 |
| | TH 18/12 | **Dropping all Courses with WP/WF** | |
| 42 | U 21/12 | Zero-Delayed Branch, Branch Target and Prediction Buffer, Dynamic Branch Prediction, 2-bit Prediction Scheme. Random Access Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM, Expanding the Data Bus Width, Increasing Memory Capacity by $2^k$. | 4.8, 5.1, 5.2 |
| | M 22/12 | **(Quiz#6)** | |
| 43 | T 23/12 | Processor-Memory Performance Gap, The Need for a Memory Hierarchy. Typical Memory Hierarchy, Principle of Locality of Reference. Basics of Caches, Block Placement: Direct Mapped. | 5.1-5.3 |
| 44 | TH 25/12 | Fully Associative Cache, Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer. Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles. | 5.1-5.4 |
| 45 | U 28/12 | CPU Time with Memory Stall Cycles, Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size. | 5.4 |