August 23, 2007

COMPUTER ENGINEERING DEPARTMENT

ICS 233

COMPUTER ARCHITECTURE & ASSEMBLY LANGUAGE

Final Exam

Summer Semester (063)

Time: 7:30-10:30 AM

Student Name : _____

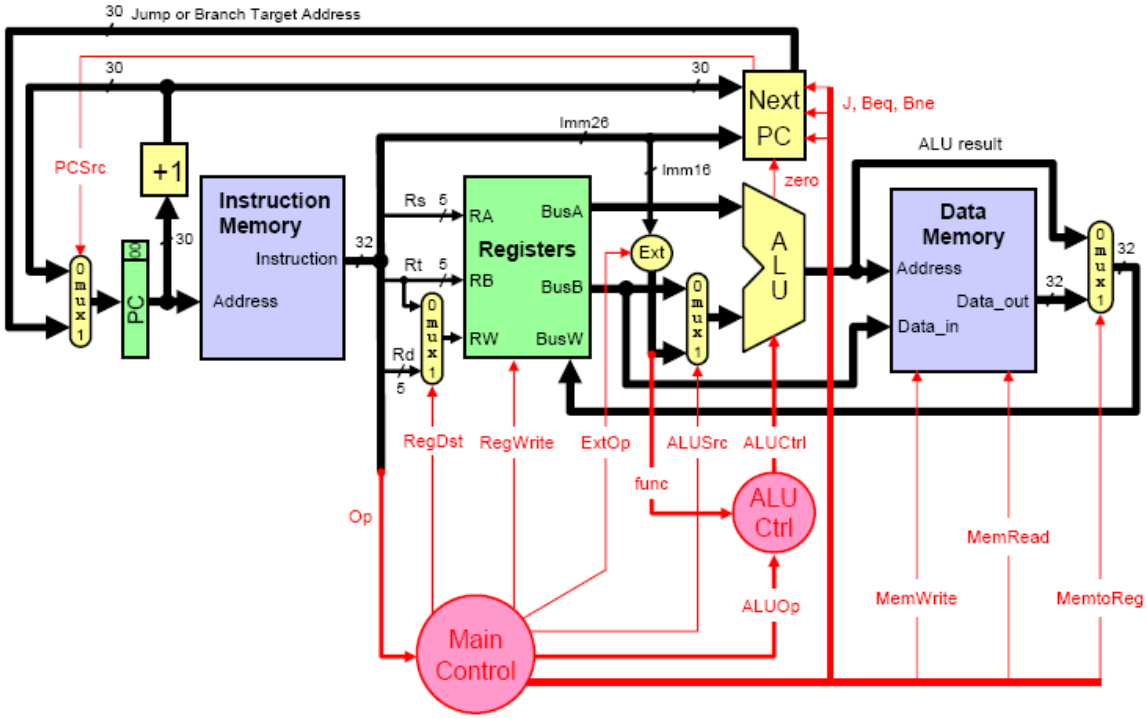
Student ID. : _____

Question	Max Points	Score
Q1	30	
Q2	14	
Q3	10	
Q4	14	
Q5	18	
Q6	14	
Total	100	

Dr. Aiman El-Maleh

[30 Points]

(Q1) Consider the single-cycle datapath and control given below for the MIPS processor implementing a subset of the instruction set:



(i) Show the control signals generated for the execution of the following instructions by filling the table given below:

Op	RegDst	RegWrite	ExtOp	ALUSrc	ALUOp	Beq	Bne	J	MemRead	MemWrite	MemtoReg
R-type											
Addi											
Andi											
Lw											
Sw											
Beq											
J											

The format of these instructions is given below for your reference:

Instruction		Meaning	Format					
add	rd, rs, rt	addition	$Op^6 = 0$	rs^5	rt^5	rd^5	0	0x20
addi	rt, rs, imm^{16}	add immediate	0x08	rs^5	rt^5	imm^{16}		
andi	rt, rs, imm^{16}	and immediate	0x0c	rs^5	rt^5	imm^{16}		
lw	rt, imm^{16}(rs)	load word	0x23	rs^5	rt^5	imm^{16}		
sw	rt, imm^{16}(rs)	store word	0x2b	rs^5	rt^5	imm^{16}		
beq	rs, rt, label	branch if equal	0x04	rs^5	rt^5	imm^{16}		
j	label	jump	0x02	imm^{26}				

(ii) We wish to add the following instructions to the single-cycle datapath. Add any necessary datapath and control signals needed for the implementation of these instructions. Show only the modified and added components to the datapath. Show the values of the control signals to control the execution of each instruction.

a. jal

Instruction		Meaning	Format	
jal	label	$31=PC+4, jump	$op^6 = 3$	imm^{26}

b. blez

Instruction		Meaning	Format			
blez	rs, label	Branch if (rs<=0)	$Op^6 = 1$	rs^5	0	imm^{16}

(iii) Assume that the propagation delays for the major components used in the datapath are as follows:

- Instruction and data memories: 200 ps
- ALU and adders: 180 ps
- Register file access (read or write): 150 ps
- Main control: 50 ps
- ALU control: 30 ps

Ignore the delays in the multiplexers, PC access, extension logic, and wires. What is the cycle time for the single-cycle datapath given above?

(iv) Suppose that we want to add a variant of the lw (load word) instruction to the single-cycle datapath, which increments the index register by 4 after loading a word from memory. This instruction **lw_inc $rt, imm^{16}($rs)** corresponds to the following two instructions:

lw $rt, imm^{16}($rs)

addi $rs, $rs, 4

This instruction would be useful in array manipulation.

a. Add any necessary datapath and control signals needed for the implementation of this instruction. Show only the modified and added components to the datapath. If there are any changes needed to the register file, just indicate the required changes and add the required signals without showing its implementation. Show the values of the control signals to control the execution of this instruction.

b. Consider the following code for adding the words of an n-word Array. The procedure receives the array address in $a0 and the number of words in $a1 and returns the sum in $v0.

```
AddArray:
        xor $v0, $v0, $v0       # Array sum=0
Next:
        lw $t0, ($a0)
        addi $a0, $a0, 4
        add $v0, $v0, $t0
        addi $a1, $a1, -1
        bne $a1, $zero, Next
        jr $ra
```

Determine the instruction count as a function of the Array size, n. What will be the instruction count if the new instruction **lw_inc** is utilized in this code. Assuming that due to the implementation of this instruction, the clock cycle is increased by 5%. What will be the maximum speedup in executing the procedure with the **lw_inc** instruction?

[14 Points]

(Q2) Consider the code given below:

```
lw $2, ($1)
addi $2, $2, 1
sw $2, ($1)
addi $1, $1, 4
```

(i) Identify all the **RAW** data dependencies in the above code. Which dependencies are data hazards that will be resolved by forwarding? Which dependencies are data hazards that will cause a stall?

(ii) Using a multiple-clock-cycle graphical representation, show the instruction execution across the pipeline including forwarding paths and stalled cycles if any. How many clock cycles will be needed to execute the instructions?

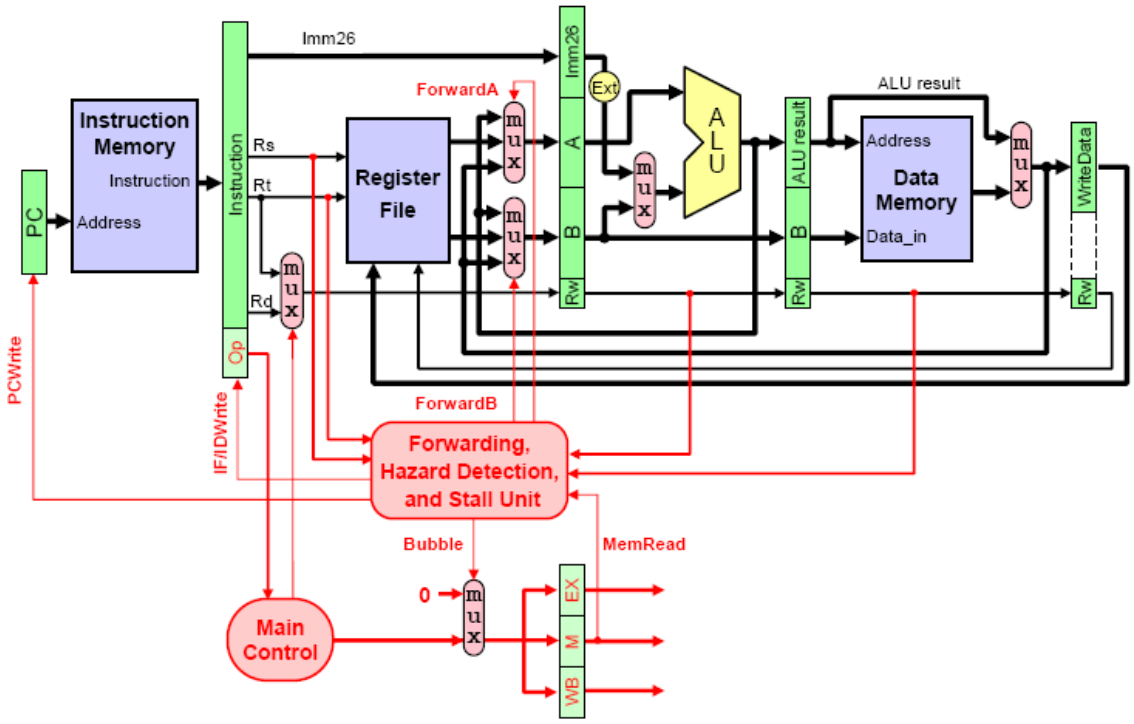
(iii) Can you modify the instructions without changing their execution behavior while reducing the number of clock cycles needed for their execution? What will be the speedup if any?

[10 Points]

(Q3) Consider the instruction sequence given below:

```
lw $t1, ($s0)
sw $t1, ($s1)
```

We can forward that data of **lw** instruction to the next **sw** instruction as required by the above example. However, such forwarding is not supported by the design given below.



(i) Show the required changes in the datapath and forwarding unit to support such forwarding.

(ii) Write the condition for generating the forwarding control signal. Identify the pipeline registers and control signals used by the **sw** and **lw** instructions when writing the condition.

[14 Points]

(Q4) Given that **TABLE** is defined as: **TABLE: .ascii "Salam Alaikom"**. The code given below counts the number of characters 'A' or 'a' found in TABLE and stores the count in register $t0.

```
        xor $t0, $t0, $t0
        li $t1, 13
        la $t2, TABLE
        addi $t2, $t2, -1
Next:   beq $t1, $zero, ENL
        addi $t2, $t2, 1
        lbu $t3, ($t2)
        ori $t3, $t3, 0x20
        li $t4, 'a'
        addi $t1, $t1, -1
        bne $t3, $t4, Next
        addi $t0, $t0, 1
        j Next
ENL:
```

(i) Show the outcomes of each of the conditional branch instructions due to the execution of the program (T for taken, N for not taken).

(ii) List the predictions and the accuracies for each of the following dynamic branch predictions schemes:

a. 1-bit prediction, initialized to **predict not taken**.

b. 2-bit predictor, initialized to **weakly predict not taken**.

[18 Points]

(Q5) Consider the following series of address references given as 16-bit addresses:

0x0000, 0x0001, 0x0002, 0x0040, 0x0041, 0x0000, 0x0001, 0x0002, 0x0040, 0x0041, 0x0042, 0x0062, 0x0063, 0x0043, 0x0045, 0x0046.

(i) Assuming a 32-byte cache organized as a **direct-mapped** cache with 4-byte block size, determine the number of bits in the offset, index and tag fields. Starting with an empty cache, show the offset, index and tag for each address reference in the list and indicate whether it is a hit or a miss. What is the miss ratio for this sequence on this cache?

Offset = Index = Tag=

Address	Tag	Index	Offset	Hit/Miss
0x0000				
0x0001				
0x0002				
0x0040				
0x0041				
0x0000				
0x0001				
0x0002				
0x0040				
0x0041				
0x0042				
0x0062				
0x0063				
0x0043				
0x0045				
0x0046				

Miss ratio =

(ii) Assuming a 32-byte cache organized as a **two-way set associative** cache with 4-byte block size, determine the number of bits in the offset, index and tag fields. Starting with an empty cache, show the offset, index and tag for each address reference in the list and indicate whether it is a hit or a miss. Assume that a FIFO replacement policy is used. What is the miss ratio for this sequence on this cache?

Offset = Index = Tag=

Address	Tag	Index	Offset	Hit/Miss
0x0000				
0x0001				
0x0002				
0x0040				
0x0041				
0x0000				
0x0001				
0x0002				
0x0040				
0x0041				
0x0042				
0x0062				
0x0063				
0x0043				
0x0045				
0x0046				

Miss ratio =

[14 Points]

(Q6) A processor runs at 2 GHz and has a CPI=1.5 for a perfect cache (i.e. without including the stall cycles due to cache misses). Assume that load and store instructions are 20% of the instructions. The processor has an I-cache with a 3% miss rate and a D-cache with 5% miss rate. The hit time is 1 clock cycle. Assume that the time required to transfer a block of data from the RAM to the cache, i.e. miss penalty, is 50 ns.

(i) What is the average memory access time for instruction access in clock cycles?

(ii) What is the average memory access time for data access in clock cycles?

(iii) What is the number of stall cycles per instruction and the overall CPI?

(iv) A new technology is proposed that can make the processor run at 4 GHz. The only impact of this technology is that the cache size has to be decreased to keep a hit time of one clock cycle increasing the I-cache miss rate to 4% and the D-cache miss rate to 6%. Assume that the time required to transfer a block of data from the RAM to the cache is still 50 ns. Will the processor be faster using the new technology? What do you suggest to increase the speedup using the new technology?