

COE 301/ICS 233, Term 172

Computer Architecture & Assembly Language

HW# 5

- Q.1.** You are required to design a combinational logic block to be used for implementing the SLL instruction for shifting an operand left by a maximum of 31 bits. Assume that the shifter will get the operand to be shifted along with the 5 bits that determine the shift amount. Design the left shifter to minimize its area and delay. Hint: use 4x1 MUXs and 2x1 MUX to implement the left shifter.
- Q.2.** Describe the effect that a single stuck-at-0 fault (i.e., the signal is always 0 regardless of what it should be) would have for the signals shown below, in the single cycle Datapath. Which instructions, if any, will not work correctly? Explain why. Consider each of the following faults separately:
- (i) RegWrite = 0
 - (ii) RegDst = 0
 - (iii) ALUSrc = 0
 - (iv) MemtoReg = 0
- Q.3.** Consider the single-cycle datapath. A friend is proposing to modify this single-cycle datapath by eliminating the control signal MemtoReg. The multiplexor that has MemtoReg as an input will instead use either the ALUSrc or the MemRead control signal. Will your friend's modification work? Can one of the two signals (MemRead and ALUSrc) substitute for the other? Explain.
- Q.4.** We wish to add the following instructions to the single-cycle datapath. Add any necessary datapath and control signals needed for the implementation of these instructions. Show only the modified and added components to the datapath. Show the values of the control signals to control the execution of each instruction.
- (i) sll
 - (ii) sllv
 - (iii) lui
 - (iv) bltz
 - (v) bgez
 - (vi) slti
 - (vii) jr