KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 301 Computer Organization

ICS 233 Computer Architecture & Assembly Language

Term 172 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | U21/1 | Syllabus and Course Introduction. Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields. | Chapter 1: Computer Abstractions and Technology  1.1-1.5 |
| 2 | T 23/1 | Instruction Fields, Advantages of High-Level Languages. Why Learn Assembly Language? Assembly vs. High-Level Languages. Assembly Language Programming Tools. Assemble and Link Process. | Chapter 1: Computer Abstractions and Technology  1.1-1.5 |
| 3 | TH 25/1 | Components of a Computer System, Memory, Address Space. Address, Data, and Control Bus. Memory Devices: RAM, DRAM, SRAM, ROM. Magnetic Disk Storage. | Chapter 1: Computer Abstractions and Technology  1.1-1.5 |
| 4 | U 28/1 | Processor-Memory Performance Gap, Memory Hierarchy, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. Technology Improvements. Overview of the MIPS Processor. | Chapter 1: Computer Abstractions and Technology  1.1-1.5 |
| 5 | T 30/1 | Overview of the MIPS Processor. MIPS General-Purpose Registers, Conventions, Instruction Formats. Assembly Language Statements, Instructions, Comments, Program Template. Data Definition Statement. Data directives, Examples of Data Definitions. Memory Alignment. | Chapter 2: Instructions: Language of the Computer (2.1-2.6) |
| 6 | TH 1/2 | Byte Ordering, Big & Little Endians. System Calls. **(Quiz#1)** | Appendix A.9-A.10 |
| 7 | U 4/2 | System Calls, Sum of Three Integers Program. Case Conversion Program. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions. | Appendix A.9-A.10 |
| 8 | T 6/2 | Integer Storage Sizes. Binary and Hexadecimal Addition. Signed Integers and 2's Complement Notation. Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction. Ranges of Signed Integers. Carry and Overflow. | Chapter 1: Computer Abstractions and Technology  1.1-1.5 |
| 9 | TH 8/2 | Character representation.Overview of the MIPS Processor. MIPS General-Purpose Registers, Conventions, Instruction Formats. Instruction Categories. Integer Add /Subtract Instructions,Logical Bitwise Instructions: AND, OR, XOR, NOR. Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of shift instructions in performing multiplication and division. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 10 | U 11/2 | Use of shift instructions in performing multiplication and division I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. Multiplication and Division Instructions. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 11 | T 13/2 | Multiplication and Division Instructions. Conditional Branch Instructions. Translating an IF Statement. Compound Expression with AND, Compound Expression with OR. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 12 | TH 15/2 | Conditional Branch Instructions. Set on Less Than Instructions, Pseudo-Instructions. Signed & Unsigned Comparison. Arrays, Static Array Allocation, Dynamic Memory Allocation, Computing the Addresses of Elements in a one-dimensional array. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 13 | U 18/2 | Computing the Addresses of Elements in a two-dimensional array. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword. Translating a WHILE Loop. Using Pointers to Traverse Arrays. | Chapter 2: Instructions: Language of the Computer (2.1-2.7) |
| 14 | T 20/2 | Copying a String, Initializing a Column of a Matrix, Addressing Modes. Functions, Function Call and Return Instructions. | Chapter 2: Instructions: Language of the Computer (2.8) |
| 15 | TH 22/2 | Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. Parameter Passing, Stack Frame. **(Quiz#2)** | Chapter 2: Instructions: Language of the Computer (2.8) |
| 16 | U 25/2 | Parameter Passing, Stack Frame, Preserving Registers. | Chapter 2: Instructions: Language of the Computer (2.8) |
| 17 | T 27/2 | Allocating a Local Array on the Stack, Bubble Sort, Example of a Recursive Function. | Chapter 2: Instructions: Language of the Computer (2.8) |
| 18 | TH 1/3 | **(Quiz#3)** |  |
|  | TH 1/3 | **Last Day for Dropping with W** |  |
| 19 | U 4/3 | Floating-Point Numbers, Floating-Point Representation. IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation. Converting FP Decimal to Binary. | Chapter 3: Arithmetic for Computers (3.5) |
| 20 | T 6/3 | Largest & Smallest Normalized Float. Zero, Infinity, and NaN, Denormalized Numbers. Floating-Point Comparison. Simple 6-bit Floating Point Example. Floating Point Addition/Subtraction. | Chapter 3: Arithmetic for Computers (3.5) |
| 21 | TH 8/3 | Floating Point Addition/Subtraction. Floating Point Adder Block Diagram. Floating Point Multiplication, Extra Bits to Maintain Precision**.** | Chapter 3: Arithmetic for Computers (3.5) |
| 22 | U 11/3 | Guard Bit, Round and Sticky bits. IEEE 754 Rounding Modes. **(Quiz#4)** | Chapter 3: Arithmetic for Computers (3.5) |
| 23 | T 13/3 | IEEE 754 Rounding Modes. MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions. Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives. | Chapter 3: Arithmetic for Computers (3.5)  4.1-4.3 |
| 24 | TH 15/3 | FP Syscall Services. Example: Area of a circle. Matrix Multiplication. Single Cycle Processor Design: Designing a Processor: Step-by-Step. Review of MIPS Instruction Formats, Register Transfer Level (RTL). Instructions Executed in Steps. | Chapter 3: Arithmetic for Computers (3.5)  4.1-4.3 |
| 25 | U 18/3 | Instructions Executed in Steps, Requirements of the Instruction Set. Components of the Datapath. Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File. Building a Multifunction ALU. | 4.1-4.3 |
| 26 | T 20/3 | Building a Multifunction ALU. **(Quiz#5)** | 4.1-4.3 |
| 27 | TH 22/3 | Shifter Design. | 4.1-4.3 |
|  | S 24/3 | **Midterm Exam** |  |
| 28 | U 25/3 | Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew. Instruction Fetching Datapath, Datapath for R-type Instructions. Datapath for I-type ALU Instructions, Combining R-type & I-type Datapaths, Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store. | 4.1-4.4 |
| 29 | T 27/3 | Adding Jump and Branch instructions to Datapath. | 4.1-4.4 |
| 30 | TH 29/3 | Main Control, ALU Control, PC Control. | 4.1-4.4 |
|  | TH 29/3 | **Last Day for Dropping all Courses with W** |  |
| 31 | U 1/4 | Review of control unit design. Worst Case Timing (Load Instruction). Design of other instructions: jr, lui, jal. | 4.1-4.4 |
| 32 | T 3/4 | What is Performance? Factors affecting execution time. Response Time and Throughput, Definition of Performance, CPU Execution Time, Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation. Factors Impacting Performance. | 1.6 |
| 33 | TH 5/4 | Factors Impacting Performance. Determining the CPI. Performance Comparison Examples. Amdahl’s Law. | 1.6 |
| 34 | U 8/4 | Amdahl’s Law. Benchmarks, The SPEC CPU2006 Benchmarks. Performance and Power. Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining. | 1.6 & 4.5-4.6 |
| 35 | T 10/4 | Pipelined Datapath. Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance. Pipelined Control. | 4.6-4.8 |
| 36 | TH 12/4 | Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards. Implementing Forwarding. | 4.8 |
| 37 | U 15/4 | No Class |  |
| 38 | T 17/4 | **(Quiz#6)** |  |
| 39 | TH 19/4 | Implementing Forwarding. RAW Hazard Detection. Forwarding Unit. Load Delay, Detecting RAW Hazard after Load. Hazard Detection and Stall Unit. | 4.8 |
|  | S 21/4  (Make up) | Hazard Detection and Stall Unit, Compiler Scheduling to reduce LW Stalls, Handling Control Hazards. | 4.8 |
| 40 | U 22/4 | Random Access Memory, Typical Memory Structure, Static RAM Storage Cell. Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM. Expanding the Data Bus Width, Increasing Memory Capacity by 2k. Processor-Memory Performance Gap. Principle of Locality of Reference. | 5.1-5.3 |
| 41 | T 24/4 | Block Placement: Direct Mapped. Fully Associative Cache, Set-Associative Cache. | 5.1-5.4 |
| 42 | TH 26/4 | Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer. What happens with a cache miss. | 5.1-5.4 |
|  | TH 26/4 | **Dropping all Courses with WP/WF** |  |
| 43 | U 29/4 | Replacement Policy. Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles, Average Memory Access Time. | 5.1-5.4 |
| 44 | T 1/5 | Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity**. (Quiz#7)** | 5.1-5.4 |
| 45 | TH 3/5 | Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size. Review for Final Exam. | 5.1-5.4 |