KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 301 Computer Organization
ICS 233 Computer Architecture & Assembly Language

Term 171 Lecture Breakdown

Lec#	Date	Topics	Ref.
1	U17/9	Syllabus and Course Introduction.	
2	T 19/9	Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages. Why Learn Assembly Language? Assembly vs. High-Level Languages.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
3	TH 21/9	Assembly Language Programming Tools. Assemble and Link Process, Components of a Computer System, Memory, Address Space. Address, Data, and Control Bus.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
	U 24/9	**National Day Holiday**	
4	T 26/9	Memory Devices: RAM, DRAM, SRAM, ROM. Memory Interleaving. Magnetic Disk Storage, Processor-Memory Performance Gap.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
5	TH 28/9	Memory Hierarchy, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. Technology Improvements. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
6	U 1/10	Integer Storage Sizes. Binary and Hexadecimal Addition. Signed Integers and 2's Complement Notation. Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction. Ranges of Signed Integers. Carry and Overflow.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
7	T 3/10	Character representation, parity bit. Overview of the MIPS Processor. MIPS General-Purpose Registers, Conventions, Instruction Formats. Instruction Categories.	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
8	TH 5/10	Integer Add /Subtract Instructions, Logical Bitwise Instructions: AND, OR, XOR, NOR. **(Quiz#1)**	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
9	S 7/10	NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of shift instructions in performing multiplication and division. I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. J-Type Format. Conditional Branch Instructions. Set on Less Than Instructions.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
10	U 8/10	Conditional Branch Instructions. Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement. Compound Expression with AND,	Chapter 2: Instructions:

		Compound Expression with OR, Signed & Unsigned Comparison.	Language of the Computer (2.1-2.7)
11	T 10/10	Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword. Translating a WHILE Loop. Using Pointers to Traverse Arrays. Copying a String. Summing an Integer Array.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
12	TH 12/10	Addressing Modes, Branch / Jump Addressing Jump and Branch Limits, PC-Relative Addressing. Summary of RISC Design. Assembly Language Statements, Instructions, Comments, Program Template. Data Definition Statement. Data directives, Examples of Data Definitions.	2.10, Appendix A.9-A.10
13	U 15/10	Memory Alignment. Byte Ordering, Big & Little Endians. System Calls, Sum of Three Integers Program. Case Conversion Program. File operations. Introduction to Procedures.	Appendix A.9-A.10
14	T 17/10	Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. Parameter Passing, Stack Frame, Preserving Registers. Selection Sort Procedure.	Chapter 2: Instructions: Language of the Computer (2.8)
15	TH 19/10	Selection Sort Procedure. Recursive Procedures: factorial. Unsigned Multiplication Hardware, Signed Multiplication.	Chapter 3: Arithmetic for Computers (3.3)
	S 21/10	**Major Exam I**	
16	U 22/10	Signed Multiplication Hardware, Fast Multiplication, Unsigned Division. Division Algorithm & Hardware. Signed Division, Multiplication and Division in MIPS. Integer to String Procedure.	Chapter 3: Arithmetic for Computers (3.3-3.4)
17	T 24/10	Integer to String Procedure. Floating-Point Numbers, Floating-Point Representation. IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation.	Chapter 3: Arithmetic for Computers (3.4-3.5)
18	TH 26/10	, Biased Exponent Representation. Converting FP Decimal to Binary. Largest & Smallest Normalized Float. Zero, Infinity, and NaN, Denormalized Numbers. Floating-Point Comparison.	Chapter 3: Arithmetic for Computers (3.5)
	TH 26/10	**Last Day for Dropping with W**	
19	U 29/10	Simple 6-bit Floating Point Example. Floating Point Addition/Subtraction. Floating Point Adder Block Diagram.	Chapter 3: Arithmetic for Computers (3.5)
20	T 31/10	Floating Point Adder Block Diagram, Floating Point Multiplication, Extra Bits to Maintain Precision**. (Quiz#2)**	Chapter 3: Arithmetic for Computers (3.5)
21	TH 2/11	Guard Bit, Round and Sticky bits. IEEE 754 Rounding Modes.	Chapter 3: Arithmetic for Computers (3.5)
22	U 5/11	MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions. Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle. Single Cycle Processor Design: Designing	Chapter 3: Arithmetic for Computers (3.5) 4.1-4.3

		a Processor: Step-by-Step. Review of MIPS Instruction Formats, Register Transfer Level (RTL). Instructions Executed in Steps, Requirements of the Instruction Set. Components of the Datapath.	
23	T 7/11	Components of the Datapath. **(Quiz#3)**	4.1-4.3
24	TH 9/11	Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File. Building a Multifunction ALU.	4.1-4.3
25	U 12/11	Shifter Design, Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew. Instruction Fetching Datapath, Datapath for R-type Instructions. Datapath for I-type ALU Instructions, Combining R-type & I-type Datapaths, Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store.	4.1-4.4
26	T 14/11	Adding Jump and Branch to Datapath. Controlling the Execution of Jump & Branch**.** Main Control.	4.1-4.4
27	TH 16/11	Main Control. **(Quiz#4)**	4.1-4.4
28	U 19/11	ALU Control, Worst Case Timing (Load Instruction). Design of other instructions: jr, sll, sllv, lui, jgez, jgtz.	4.1-4.4
29	T 21/11	What is Performance? Factors affecting execution time. Response Time and Throughput, Definition of Performance, CPU Execution Time, Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation. Factors Impacting Performance.	1.6
30	TH 23/11	Factors Impacting Performance. Determining the CPI. Performance Comparison Examples. Amdahl's Law.	1.6
	TH 23/11	**Last Day for Dropping all Courses with W**	
31	U 26/11	Amdahl's Law. Benchmarks, The SPEC CPU2000 Benchmarks. Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining.	1.6 & 4.5-4.6
32	T 28/11	**(Quiz#5)**	
33	TH 30/11	Review for Major Exam II.	
	S 2/12	**Major Exam II**	
34	U 3/12	Pipelined Datapath. Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance. Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards.	4.6-4.8
35	T 5/12	Implementing Forwarding. RAW Hazard Detection. Forwarding Unit.	4.8
36	TH 7/12	Forwarding Unit. Load Delay, Detecting RAW Hazard after Load. Hazard Detection and Stall Unit.	4.8
37	U 10/12	Hazard Detection and Stall Unit. Compiler Scheduling, Reducing the Delay of Branches. Branch Hazard Alternatives, Delayed Branch.	4.8
38	T 12/12	**(Quiz#6)**	

39	TH 14/12	Branch Hazard Alternatives, Delayed Branch. Zero-Delayed Branch, Branch Target and Prediction Buffer.	4.8
40	U 17/12	Dynamic Branch Prediction, 1-bit & 2-bit Prediction Scheme. Random Access Memory, Typical Memory Structure, Static RAM Storage Cell.	4.8, 5.1-5.3
41	T 19/12	Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM. Expanding the Data Bus Width, Increasing Memory Capacity by 2^k. Processor-Memory Performance Gap. Principle of Locality of Reference.	5.1-5.3
42	TH 21/12	Block Placement: Direct Mapped. Fully Associative Cache, Set-Associative Cache. Write Policy.	5.1-5.4
	TH 21/12	**Dropping all Courses with WP/WF**	
43	U 24/12	Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer. Replacement Policy.	5.1-5.4
44	T 26/12	Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles, Average Memory Access Time. Improving Cache Performance, Types of Cache Misses: Compulsory, Conflict and Capacity.	5.1-5.4
45	TH 28/12	Average Memory Access Time. Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size.	5.1-5.4