KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 301 Computer Organization
ICS 233 Computer Architecture & Assembly Language

Term 161 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	U18/9	Syllabus and Course Introduction.	
2	T 20/9	Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
	TH 22/9	National Day Holiday	
3	U 25/9	Why Learn Assembly Language? Assembly vs. High-Level Languages, Assembly Language Programming Tools. Assemble and Link Process, Components of a Computer System, Memory, Address Space. Address, Data, and Control Bus.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
4	T 27/9	Memory Devices: RAM, DRAM, SRAM, ROM. Memory Interleaving.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
5	TH 29/9	Magnetic Disk Storage, Processor-Memory Performance Gap. Memory Hierarchy, Processor: Datapath, Control, Program Counter.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
6	U 2/10	Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. Technology Improvements. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions. Integer Storage Sizes. Binary and Hexadecimal Addition. Signed Integers and 2's Complement Notation.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
7	T 4/10	Signed Integers and 2's Complement Notation, Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction. Ranges of Signed Integers. Carry	Chapter 2: Instructions: Language of the Computer (2.1-2.2)

		and Overflow. Character representation, parity bit. Overview of the MIPS Processor.	
8	TH 6/10	MIPS General-Purpose Registers, Conventions, Instruction Formats. Instruction Categories. Instruction Categories. R-Type Arithmetic, Logical, and Shift Instructions, Integer Add /Subtract Instructions.	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
9	U 9/10	Logical Bitwise Instructions: AND, OR, XOR, NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of shift instructions in performing multiplication and division.	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
10	T 11/10	I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. **(Quiz#1)**	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
11	TH 13/10	J-Type Format. Conditional Branch Instructions. Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
12	U 16/10	Compound Expression with AND, Compound Expression with OR, Signed & Unsigned Comparison. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword. Translating a WHILE Loop. Using Pointers to Traverse Arrays.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
13	T 18/10	Using Pointers to Traverse Arrays. Copying a String. Summing an Integer Array. Addressing Modes, Branch / Jump Addressing Jump and Branch Limits, PC-Relative Addressing. Summary of RISC Design.	2.10
14	TH 20/10	Assembly Language Statements, Instructions, Comments, Program Template. Data Definition Statement. Data directives, Examples of Data Definitions, Memory Alignment. Byte Ordering, Big & Little Endians.	Appendix A.9-A.10
	S 22/10	**Major Exam I**	
15	U 23/10	System Calls, Sum of Three Integers Program. Case Conversion Program. File operations. Introduction to Procedures.	Appendix A.9-A.10
16	T 25/10	Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. Parameter Passing, Stack Frame, Preserving Registers.	Chapter 2: Instructions: Language of the Computer (2.8)
17	TH 27/10	Parameter Passing, Stack Frame, Preserving Registers. Selection Sort Procedure. Recursive Procedures: factorial.	Chapter 2: Instructions: Language of the Computer (2.8)
	TH 27/10	**Last Day for Dropping with W**	

18	U 30/10	Unsigned Multiplication Hardware, Signed Multiplication.	Chapter 3: Arithmetic for Computers (3.3)
19	T 1/11	Signed Multiplication Hardware, Fast Multiplication, Unsigned Division. Division Algorithm & Hardware.	Chapter 3: Arithmetic for Computers (3.3-3.4)
20	TH 3/11	Unsigned Division. Division Algorithm & Hardware. Signed Division, Multiplication and Division in MIPS. Integer to String Procedure.	Chapter 3: Arithmetic for Computers (3.3-3.4)
21	U 6/11	Integer to String Procedure. Floating-Point Numbers, Floating-Point Representation. IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation. Converting FP Decimal to Binary.	Chapter 3: Arithmetic for Computers (3.4-3.5)
22	T 8/11	Converting FP Decimal to Binary. Largest & Smallest Normalized Float. **(Quiz#2)**	Chapter 3: Arithmetic for Computers (3.5)
23	TH 10/11	Zero, Infinity, and NaN, Denormalized Numbers. Floating-Point Comparison. Simple 6-bit Floating Point Example. Floating Point Addition/Subtraction.	Chapter 3: Arithmetic for Computers (3.5)
	13-17 Nov.	Mid-Term break	
24	U 20/11	Floating Point Addition/Subtraction, Floating Point Adder Block Diagram. Floating Point Multiplication.	Chapter 3: Arithmetic for Computers (3.5)
25	T 22/11	Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit. **(Quiz#3)**	Chapter 3: Arithmetic for Computers (3.5)
26	TH 24/11	Guard Bit, Round and Sticky bits. IEEE 754 Rounding Modes. MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions. Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle.	Chapter 3: Arithmetic for Computers (3.5)
27	U 27/11	Single Cycle Processor Design: Designing a Processor: Step-by-Step. Review of MIPS Instruction Formats, Register Transfer Level (RTL). Instructions Executed in Steps, Requirements of the Instruction Set.	4.1-4.3
28	T 29/11	Requirements of the Instruction Set. Components of the Datapath. Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File. Building a Multifunction ALU.	4.1-4.3

29	TH 1/12	Building a Multifunction ALU, Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew. Instruction Fetching Datapath, Datapath for R-type Instructions. Datapath for I-type ALU Instructions, Combining R-type & I-type Datapaths.	4.1-4.3
	TH 1/12	**Last Day for Dropping all Courses with W**	
30	U 4/12	Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store. Adding Jump and Branch to Datapath. Controlling the Execution of Jump & Branch**.** Main Control.	4.1-4.4
31	T 6/15	Main Control. ALU Control. **(Quiz#4)**	4.1-4.4
32	TH 8/12	Worst Case Timing (Load Instruction). Review of Control Unit Design.	4.1-4.4
	S 10/12	**Major Exam II**	
33	U 11/12	What is Performance? Factors affecting execution time. Response Time and Throughput, Definition of Performance, CPU Execution Time, Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation.	1.6
34	T 13/12	Factors Impacting Performance. Determining the CPI.	1.6
35	TH 15/12	Determining the CPI. Performance Comparison Examples.	1.6
36	U 18/12	Amdahl's Law. Benchmarks, The SPEC CPU2000 Benchmarks. Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining.	1.6 & 4.5-4.6
37	T 20/12	Synchronous Pipeline, Pipeline Performance. Pipelined Datapath. Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance.	4.5-4.6
38	TH 22/12	Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards. Implementing Forwarding.	4.6-4.8
39	U 25/12	RAW Hazard Detection. Forwarding Unit. Load Delay, Detecting RAW Hazard after Load. **(Quiz#5)**	4.8
40	T 27/12	Hazard Detection and Stall Unit. Compiler Scheduling, Reducing the Delay of Branches.	4.8
41	TH 29/12	Branch Hazard Alternatives, Delayed Branch. Zero-Delayed Branch, Branch Target and Prediction Buffer. Dynamic Branch Prediction, 1-bit & 2-bit Prediction Scheme.	4.8
	TH 29/12	**Dropping all Courses with WP/WF**	

42	U 1/1	Random Access Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM. Expanding the Data Bus Width, Increasing Memory Capacity by 2^k. Processor-Memory Performance Gap. Principle of Locality of Reference.	5.1-5.3
43	T 3/1	Block Placement: Direct Mapped. Fully Associative Cache, Set-Associative Cache. Write Policy.	5.1-5.4
44	TH 5/1	Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer. Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles.	5.1-5.4
45	U 8/1	Memory Stall Cycles, CPU Time with Memory Stall Cycles. Average Memory Access Time. Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size.	5.1-5.4