KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 301 Computer Organization
ICS 233 Computer Architecture & Assembly Language

Term 151 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	U23/8	Syllabus Introduction.	
2	T 25/8	Assembly and Machine Language, Compiler and Assembler, Instructions and Machine Language, Instruction Fields, Advantages of High-Level Languages, Why Learn Assembly Language? Assembly vs. High-Level Languages, Assembly Language Programming Tools.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
3	TH 27/8	Assembly Language Programming Tools, Assemble and Link Process, Components of a Computer System, Memory, Address Space. Address, Data, and Control Bus. Memory Devices: RAM, DRAM, SRAM, ROM. Magnetic Disk Storage	Chapter 1: Computer Abstractions and Technology 1.1-1.5
4	U 30/8	Processor-Memory Performance Gap. Memory Hierarchy, Processor: Datapath, Control, Program Counter, Instruction Register, Fetch-Execute Cycle. Technology Improvements. Positional Number Systems, Binary and Hexadecimal Numbers, Base Conversions.	Chapter 1: Computer Abstractions and Technology 1.1-1.5
5	T 1/9	Base Conversions, Integer Storage Sizes. Binary and Hexadecimal Addition. Signed Integers and 2's Complement Notation, Sign Extension. Two's Complement of a Hexadecimal, Binary & Hexadecimal Subtraction.	
6	TH 3/9	Ranges of Signed Integers. Carry and Overflow. Character representation, parity bit. Overview of the MIPS, Processor, MIPS, General-Purpose Registers, Conventions	Chapter 2: Instructions: Language of the Computer (2.1-2.2)
7	U 6/9	Instruction Formats. Instruction Categories. Instruction Categories. R-Type Arithmetic, Logical, and Shift Instructions, Integer Add /Subtract Instructions. Logical Bitwise Instructions: AND, OR, XOR, NOR. **(Quiz#1)**	Chapter 2: Instructions: Language of the Computer (2.1-2.6)

8	T 8/9	Logical Bitwise Instructions: AND, OR, XOR, NOR, Shift Instructions: sll, srl sra, sllv, srlv, srav. Use of shift instructions in performing multiplication and division.	Chapter 2: Instructions: Language of the Computer (2.1-2.6)
9	TH 10/9	I-Type Format, I-Type ALU Instructions, 32-bit Constants, Applications of logical instructions. J-Type Format. Conditional Branch Instructions.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
10	U 13/9	Conditional Branch Instructions, Set on Less Than Instructions, Pseudo-Instructions. Translating an IF Statement, Compound Expression with AND.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
11	T 15/9	Compound Expression with OR, Signed & Unsigned Comparison. Load and Store Instructions: Load and Store Word, Load and Store Byte and Halfword. Translating a WHILE Loop. Using Pointers to Traverse Arrays.	Chapter 2: Instructions: Language of the Computer (2.1-2.7)
12	TH 17/9	Copying a String. Summing an Integer Array. Addressing Modes, Branch / Jump Addressing Jump and Branch Limits, PC-Relative Addressing. Summary of RISC Design.	2.10
	18/9-3/10	**Id al-Adha Vacation**	
	S 3/10	**Major Exam I**	
13	U 4/10	Assembly Language Statements, Instructions, Comments, Program Template. Data Definition Statement. Data directives, Examples of Data Definitions, Memory Alignment. Byte Ordering, Big & Little Endians. System Calls.	Appendix A.9-A.10
14	T 6/10	**(Quiz#2)**	
15	TH 8/10	System Calls, Sum of Three Integers Program. Case Conversion Program. File operations. Introduction to Procedures.	Appendix A.9-A.10
	S 10/10	**Major Exam I**	
16	U 11/10	Procedures, Call / Return Sequence, Instructions for Procedures: JAL, JR, JALR. Parameter Passing, Stack Frame, Preserving Registers. Parameter Passing, Stack Frame, Preserving Registers.	Chapter 2: Instructions: Language of the Computer (2.8)
17	T 13/10	Selection Sort Procedure. Recursive Procedures: factorial. Unsigned Multiplication Hardware, Signed Multiplication.	Chapter 3: Arithmetic for Computers (3.3)
18	TH 15/10	Signed Multiplication Hardware. Return of Major Exam I Papers.	Chapter 3: Arithmetic for Computers (3.3)

		TH 15/10	**Last Day for Dropping with W**	
19	U 18/10	Fast Multiplication, Unsigned Division. Division Algorithm & Hardware. Signed Division, Multiplication and Division in MIPS. Integer to String Procedure.	Chapter 3: Arithmetic for Computers (3.3-3.4)	
20	T 20/10	Floating-Point Numbers, Floating-Point Representation. IEEE 754 Floating-Point Standard, Normalized Floating Point Numbers, Biased Exponent Representation. Converting FP Decimal to Binary.	Chapter 3: Arithmetic for Computers (3.5)	
21	TH 22/10	Largest & Smallest Normalized Float, Zero, Infinity, and NaN, Denormalized Numbers. Floating-Point Comparison. Simple 6-bit Floating Point Example. Floating Point Addition/Subtraction.	Chapter 3: Arithmetic for Computers (3.5)	
22	U 25/10	**(Quiz#3)** Floating Point Addition/Subtraction.	Chapter 3: Arithmetic for Computers (3.5)	
23	T 27/10	Floating Point Adder Block Diagram. Floating Point Multiplication, Extra Bits to Maintain Precision, Guard Bit, Round and Sticky bits.	Chapter 3: Arithmetic for Computers (3.5)	
	T 27/10 (Makeup)	IEEE 754 Rounding Modes. MIPS Floating-Point Instructions: Arithmetic Instructions, Load/Store Instructions. Data Movement Instructions, Convert Instructions, Compare and Branch Instructions, FP Data Directives, FP Syscall Services. Example: Area of a circle.	Chapter 3: Arithmetic for Computers (3.5)	
24	TH 29/10	Single Cycle Processor Design: Designing a Processor: Step-by-Step. Review of MIPS Instruction Formats, Register Transfer Level (RTL). Instructions Executed in Steps, Requirements of the Instruction Set. Components of the Datapath.	4.1-4.3	
25	U 1/11	Register Element, MIPS Register File, Tri-State Buffers. Designing the MIPS Register File. Building a Multifunction ALU.	4.1-4.3	
26	T 3/11	**(Quiz#4)**		
27	TH 5/11	No Class.		
28	U 8/11	Building a Multifunction ALU, Instruction and Data Memories, Clocking Methodology, Determining the Clock Cycle, Clock Skew. Instruction Fetching Datapath, Datapath for R-type Instructions.	4.1-4.3	
29	T 10/11	Datapath for I-type ALU, Instructions, Combining R-type & I-type Datapaths. Controlling ALU Instructions, Details of the Extender, Controlling the Execution of Load & Store. Adding Jump and Branch to Datapath. Controlling the Execution of Jump & Branch**.**	4.1-4.3	

30	TH 12/11	Main Control. ALU Control.	4.1-4.4
	TH 12/11	**Last Day for Dropping all Courses with W**	
31	U 15/11	Worst Case Timing (Load Instruction). What is Performance? Factors affecting execution time. Response Time and Throughput, Definition of Performance, CPU Execution Time, Improving Performance. Clock Cycles per Instruction (CPI), Performance Equation. Factors Impacting Performance.	4.1-4.4 1.6
32	T 17/11	Determining the CPI.	1.6
33	TH 19/11	Amdahl's Law. Benchmarks, The SPEC CPU2000 Benchmarks. Pipelined Processor Design: Pipelining Example. Serial execution versus Pipelining.	1.6 & 4.5-4.6
	S 21/11	**Major Exam II**	
34	U 22/11	Synchronous Pipeline, Pipeline Performance. Pipelined Datapath. Instruction–Time Diagram, Single-Cycle vs. Pipelined Performance.	4.5-4.6
35	T 24/11	Pipelined Control. Pipeline Hazards, Structural Hazards, Resolving Structural Hazards, Data Hazards. Implementing Forwarding.	4.6-4.8
36	TH 26/11	No Class.	
37	U 29/11	RAW Hazard Detection. Forwarding Unit. Load Delay, Detecting RAW Hazard after Load.	4.8
38	T 1/12	Hazard Detection and Stall Unit. Compiler Scheduling. WAR Hazard, WAW Hazard. Control Hazards.	4.8
39	TH 3/12	Reducing the Delay of Branches, Branch Hazard Alternatives, Delayed Branch. Zero-Delayed Branch, Branch Target and Prediction Buffer.	4.8
	TH 3/12 Makeup	Branch Target and Prediction Buffer, Dynamic Branch Prediction, 1-bit & 2-bit Prediction Scheme.	4.8
40	U 6/12	Random Access Memory, Typical Memory Structure, Static RAM Storage Cell, Dynamic RAM Storage Cell, DRAM Refresh Cycles Trends in DRAM. Expanding the Data Bus Width, Increasing Memory Capacity by 2^k. Processor-Memory Performance Gap.	5.1-5.3
41	T 8/12	The Need for a Memory Hierarchy. Typical Memory Hierarchy. Principle of Locality of Reference. Basics of Caches, Block Placement: Direct Mapped. Fully Associative Cache.	5.1-5.3
42	TH 10/12	**(Quiz#5)**	
	TH 10/12	**Dropping all Courses with WP/WF**	

43	U 13/12	Set-Associative Cache. Write Policy, Write Miss Policy, Write Buffer.	5.1-5.4
44	T 15/12	Replacement Policy, Cache Performance and Memory Stall Cycles: Hit Rate and Miss Rate, Memory Stall Cycles, CPU Time with Memory Stall Cycles. Average Memory Access Time.	5.1-5.4
45	TH 17/12	Improving Cache Performance: Average Memory Access Time, Small and Simple Caches, Larger Size and Higher Associativity, Larger Block Size.	5.4