King Fahd University of Petroleum and Minerals
College of Computer Science and Engineering
Computer Engineering Department

Research Proposal

to seek funding under the:
SABIC Fast Track Research Grants Program

Using the On-Chip Advantage in Designing Networks-On-Chip

Proposed By:

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Abstract

In recent years the chip design methodology shifted from a circuit-centered approach to an IP-centered approach relying more on ready to use IP block to make chips that look more like systems. The name “System-on-Chip” (SoC) comes from there. In the research community, it became a consensus to use networks for inter-IP blocks communication. The current research proposal is aimed at contributing to the field of Networks on-Chip (NoCs) design methodology**.**

Many of the solutions proposed are simply borrowing the architectures and topologies from the interconnection networks for parallel architectures field and integrating them on-chip. Although many aspects directly related to the on-chip context have been addressed, like power consumption or clock distribution and synchronization (asynchronous designs), it still appears that the proposed solutions are not fully centered around the “on-chip” context. The proposed research aims at developing a design methodology that fully uses the many other advantages of on-chip context. A construction by example is followed in building the methodology.

As a first exercise of developing the methodology, we propose to adapt the Multistage Interconnection Network (MIN) topology by modifying it to fit the on-chip context. The objective is to obtain a modified topology and router architecture that presents more advantages than the one obtained by the methodology followed up to now. Clearly showing the advantages in terms of performance, size and wire routing cost will serve as a validation to the proposed methodology.

Simulation is used as an experimentation testbed. Measurement data will be collected from simulation and analyzed in order to validate the hypothesis predicted by the methodology. A simulator that will integrate all the needed features will be developed for that purpose.

The outcome of this research effort is expected to be at least one journal or conference publication along with substantial contribution to the field. A router model, written in HDL (either VHDL or Verilog), is also expected as an outcome of this project.

The budget required for this project is around 74,000 SR and its duration is 11 months.

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1. Introduction

In recent years, the activity of ASIC design converged towards producing more and more complex ASICs. The advances in technology helped in achieving that. A new design methodology aimed at making the design of complex chips more manageable changed the mindset of the designers. These ones are focusing more on the chip itself considering it as a complex system composed of many individual blocks. The details of the different blocks became the responsibility of other teams specialized in producing reusable IP (Intellectual Property) blocks. With the availability of more sophisticated IP blocks and the progress of the technology, the job of an ASIC design team changed into designing chips that look more like systems. The name SoC: System-on-a-Chip, comes from there.

To connect the different IPs, the design teams have to deal with many issues. Incompatible communication protocols from one IP block to another is a main issue. Heterogeneous bandwidth and latency requirements are also another issue.

Historically, a bus was used to connect the different blocks in a chip [1][2]. The bus architecture is characterized by a high latency[1] and a low throughput[2] both synonymous of poor performance.

Issues in connecting SoC blocks together look very similar to connecting computers together. Thus, borrowing the models, techniques, and tools from the network design field and applying them to SoC design became a research field worth of interest [35]. Networks-On-Chip is the name chosen to designate the use of on-chip interconnection networks in place of ad-hoc global wiring between the top-level IP blocks in SoCs [14][15][22][35]. There is a general consensus that the communication requirements, as well as the design flow, of billion transistor SoC are best accommodated by shared, segmented interconnection networks [35][38][22].

The research in NoCs can be classified into the following categories:

- Proposals that readapt the existing results obtained from the research area of interconnection networks for parallel processors, as suggested in [35][22].
- Router architecture discussion, especially, the output port allocation and buffering strategies is extensively present in the NoC area literature.
- Asynchronous design for NoC, either purely asynchronous with no clock or GALS[3] have been also explored. The main focus is on the inter-router links and the related circuitry.
- Complex architecture designs that integrate multi-service levels or a mixture of packet and circuit switching services.

From reviewing what has been done in this area, it clearly appears that the approach has mainly been indirect to the problem posed by interconnection between IP blocks. Although, there is a consensus about using networks inside the chip, the trend has been so far to borrow the methods and solutions from the networking and interconnection networks field without entirely taking into account the “on-chip” context. We believe that the right approach should start from the on-chip context and adapt the existing findings from the other areas to the specificities of being inside a single chip. This should not be limited to: synchronization, power consumption and wire-routing. Other aspects like: overhead, complexity, design-time reduction and absence of design limitations (no boundary for router I/Os). The on-chip context offers more advantages than the inter-chip context. Determinism of communication, locality of nodes (all nodes are local) and versatility of

[1] This is due to a relatively large waiting time before the bus is granted

[2] Electrical characteristics of shared bus technology limit the throughput compared to point-to-point communications

[3] Globally Synchronous Locally Asynchronous, see [GALS Thesis] for more information.

available components (the network elements are hardware models that can be parameterized and changed and are not physical components that are fixed and cannot be changed).

The contributions found in the literature review are mostly presenting a model of networks based on the use on a single topology, single routing algorithm and a single router model in the same chip. This is a constraint that solutions in the networking or the interconnection networks fields had to enforce. In the networking field:

- Routers are hardware devices (chips or boards) that are fixed and produced before deployment. Adding more ports to a router is synonymous to designing and producing a new one
- Different topologies can be implemented in function of the characteristics of the available equipment (routers). Hence, some topologies are not always possible to implement because of limitations either in the available equipment architecture or incompatibility of the equipment with the routing algorithm used by the topology. Another major limitation is that topologies are connected manually and connections depend on human intervention.

In the on-chip context, routers are fixed simultaneously as the network interface, the possible topologies, the routing algorithms and the entire chip itself. Also, routers are not general purpose in the chip context and are designed to implement the network of the chip they are going to be carried on. Thus, highly parameterized router models should be the trend in NoC design. It is then possible to integrate many router architectures on the same chip and make them cooperate to implement the NoC.

The overhead is another issue of NoC design. The network is integrated to connect between the different entities of a SoC. Its vocation is transparency to the rest of the entities. So, the overhead in terms of area or power consumption should be minimal. Overhead minimization starts at the network topology, goes all the way through the router architecture and ends at the link circuitry.

We are proposing to follow a top-down approach to the problem of NoC design. This approach starts from identifying the on-chip context. It continues by truly and efficiently adapting the existing network topologies, routing algorithms and router designs to the on-chip context. Ideas like buffer-less router architecture to minimize overhead or centralized global flow-control to eliminate data contention that are impossible in the context of classical interconnection networks become possible solutions in the on-chip context.

The benefits to the NoC design community are numerous and include defining a methodology to transform existing interconnection networks solutions to NoCs. This can lead to a more streamlined design process that can later be completely automated as it is the case for chip place and route. In this picture, the CAD tool, will, under the supervision of the designer, pick and parameterize the right router models and the right topology that fits the communication requirements of the client entities that form the SoC.

2. Literature Review

Since [22], many solutions have been proposed in the NoC area. The majority of these solutions are built by directly deriving already existing topologies and routing algorithms [21][26][33][34]. The intensive study of interconnection networks in the 80s/90s for the purpose of connecting parallel processors produced many solutions that are adapted now for the NoC area [4]-[13].
Some other proposals focus only on the router architecture alone neglecting the other components of the network like the topology, the flow control and the routing scheme. Those components do affect performances. In this perspective, many papers propose to discuss the design and

implementation constraints of the router alone following many different approaches and goals [26][29].

Another aspect of SoC IP connectivity is clock distribution and skew. In future designs it will be almost impossible to have a single clock for the entire chip [3][18][19][20][35]. Based on this, many NoC proposals went on the path of asynchronous design to achieve connectivity without the pain of synchronization. The number of contributions spans from simple asynchronous circuits [24], asynchronous router architectures [20][31] to complete asynchronous design of networks [17][18][23].

Up to here, these proposals did not provide a dramatic improvement in the performances of the networks as known in the inter-chip interconnection networks. For instance, many papers present a throughput around 40% to 50% [25][33][34]. This led some researchers to propose a mixture of operating modes and service levels to overcome the limitations in throughput inherent to wormhole networks and to provide a guarantee on the latency, very important when transmitting time-sensitive data. This way, many solutions present a mixture between packet switching, used for a "slow" path and circuit switching used for a "fast" path [18]. Some other proposals defined networks offering multiple service levels [19].

Repeating the same network topologies and routing algorithms as in inter-chip interconnection network does not fully take advantage of the on-chip property. In the inter-chip interconnection networks context, the designers were limited in the number of I/O ports they can use. This is not the case anymore for NoCs. It makes it a real advantage that has not been stressed enough in the presented solutions. This might be due to an apparent contradiction of goals between the aimed reduction in wire routing versus high-radix routers that goes against the goal of reduction in wires. Despite that, high-radix router architectures are finding serious advocates [28].

The complexity of routers did not change significantly compared to inter-chip communications. The router designs for NoCs present a complexity comparable to that of their counterparts designed for inter-chip interconnection networks [16][19][20][21][25][29][31][33][34]. In fact, these routers have been designed to fit mainly on a single chip. However, the routers in the NoC paradigm are normally designed so that several instances can easily be integrated on-chip with a relatively negligible overhead [35]. Although advances in chip technology makes it easier to achieve integration of a large amount of routers on-chip, networks built using complex, high gate-count routers will quickly suffer scalability limitations. This, without considering the overhead that may reach levels that are not negligible anymore.

3. Project Objectives

The development of a methodology for efficiently taking advantage of the "on-chip" context needs lots of experimentation and tuning. The development of a methodology for efficiently designing NoCs requires an illustrative proof that will help refine it and mature it. The goal of our research in this project is not directly to develop the methodology from scratch but to help build it by showing an illustrative example. Modifying a typical network topology and showing that by following this methodology better characteristics can be attained is the main objective of this research effort.

We choose to start with the development of a new class of NoCs based on the Multistage Interconnection Network topology [5]-[13]. MINs are well known in the literature and have been extensively studied in the past. The main goal is to arrive to a sister topology based on a family of routers that presents better parameters compared to the original MINs.

4. Description of the proposed research

The research investigation is planned for a period of 11 calendar months starting from the time of approval of the project. The project is divided into nine (09) different tasks. In section 5 below, Table 1 shows the timetable of the project and each task's place in the schedule.

The principal investigator and the two co-investigators will be working for the whole duration of the project. Two graduate students (graduate assistants or research assistants) will assist also for the entire duration of the project.

The means and methods followed to build a MIN-based NoC are formed of many steps. The seven tasks needed to complete the project are given below:

1. Analysis of the MIN in the context of on-chip design needs to be performed. The analysis findings will lead to the design of a modified topology that will present characteristics adapted to the "on-chip" context. The modified topology needs to be validated by simulation.
2. Design of the router architecture that will efficiently take advantage of the "on-chip" context in terms of latency, throughput and size.
3. Development of a cycle accurate simulator which should have the following properties:
    - Cycle accurate
    - C-based, for simplicity of development
    - Integrate the router and topology model.
    - Capable of performing measurements to document simulation outcomes
    - Modular to be easily modified and to easily integrate new models
4. Use of the simulator to perform simulations of many topology sizes and router architectures
5. Evaluation of the clocking strategy by comparing two options: single clock domain for the network separate from the other clock domains or multiple clock domains dividing the network into synchronization islands.
6. Study of the appropriate flow control and buffering strategy.
7. Performance evaluation in terms of:
    - Latency
    - Throughput
    - Area
    - Wiring complexity
    - Power consumption
- Design and verification complexity
8. Development of a parameterized router model in HDL (either VHDL or Verilog)
9. Generation of periodic and final project reports and authoring of publications for conferences/journals.

5. Project Management and Scheduling

The principal investigator along with the two co-investigators will take responsibility of the overall management of the project. The students will be computer/electrical engineering graduates with good background in computer architecture, networking, parallel architectures and digital circuit design and will work under the guidance of the investigators. Frequent meetings between the investigators and the investigators and the students shall be conducted.

The project's timetable is given in Table 1 below. It shows the scheduling of each task within the project duration. Time is expressed in months and will start as soon as the project is approved.

Table 1 – Project Time Table

Tasks	Months										
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**
Task 1											
Task 2											
Task 3											
Task 4											
Task 5											
Task 6											
Task 7											
Task 8											
Task 9											

Table 2 below shows how the tasks will be distributed among team members.

Table 2 – Task Distribution Among Team Members

Tasks	Involved Team Member(s)	Quality	Percentage Involved
Task 1	Dr. Abdelhafid Bouhraoua	PI	100%
Task 2	Dr. Abdelhafid Bouhraoua	PI	60 %
	Dr. Muhammad El-Rabaa	Co-I	40 %
Task 3	Dr. Abdelhafid Bouhraoua	PI	20 %
	Dr. Muhammad Mudawar	Co-I	30 %
	Graduate Student	-	50 %
Task 4	Dr. Abdelhafid Bouhraoua	PI	10 %
	Dr. Muhammad Mudawar	Co-I	10 %
	Graduate Students	-	80 %
Task 5	Dr. Muhammad El-Rabaa	Co-I	100 %
Task 6	Dr. Muhammad El-Rabaa	Co-I	60 %
	Dr. Abdelhafid Bouhraoua	PI	40 %
Task 7	Dr. Muhammad El-Rabaa	Co-I	60 %
	Dr. Abdelhafid Bouhraoua	PI	40 %
Task 8	Dr. Muhammad Mudawar	Co-I	20 %
	Dr. Abdelhafid Bouhraoua	PI	20 %
	Graduate Students	-	60 %
Task 9	Dr. Abdelhafid Bouhraoua	PI	40 %
	Dr. Muhammad Mudawar	Co-I	30 %
	Dr. Muhammad El-Rabaa	Co-I	30 %

6. Equipment Requirements

The requirements in terms of equipment for this project are listed below:

- Two relatively powerful PCs on which simulations will be run and that will be used as the platform for the projects. These PCs should preferably be located in a common

location where they can be easily accessed by team members. The PCs are required because for a good project management practice and for efficiency reasons, there should be at least two PC exclusively dedicated to the project.

- The Active HDL, RTL design suite software package from Aldec. The development of a parameterized router architecture requires an integrated design environment for hardware description. Many vendors offer software packages that are suitable for our task. However, after a quick search, we found that the Aldec package offers the best quality over price ratio and is the most praised in by its users that particularly acclaimed its customer support as being excellent.

7. Monitoring and Evaluation Plan

Usual project management tools will be followed in monitoring the progress of the project. Evaluating the findings and obtained results will be carried out through benchmarking against previously published work.

8. Deliverables

Several items are expected to be delivered as a result of this research effort:

1. A research report that will present the findings that will be reached after the completion of the project
2. At least one conference or journal paper published in a good standing conference or journal.
3. Router HDL (VHDL or Verilog) parameterized model adapted to the modified MIN in the “on-chip” context.
4. Training of graduate students in advanced computer architecture, performance evaluation, simulator development, and implementation issues.
5. The results of this work can be utilized in designing complete systems on a chip (SoC). By making the design of the network-on-chip ubiquitous, doors are going to be open for quicker design of complete systems.
6. This experience can be utilized to establish a local highly skilled SoC design center that will be distinguished by its methodology that helps slash SoC project schedules. By reducing the complexity and overhead of the NoC as well as increasing its performances, SoC design expertise can be attained.
7. The results of this work can be used by other investigators in academia and industry as basis for more research on digital data communication techniques.

9. Utility Value of the Project

The results obtained from the current research proposal may be used as a basis for another effort that will concentrate on building the methodology of NoC design in the on-chip context. The aim is to arrive at the definition of the methodology that will be the basis for Automated Design Tools and possibly develop a technology enabler or demonstration tool as part of the future project. Journal and/or conference publications are also another way of using the findings of this project. Also, possible patents of the methodology itself are worth of exploration.

10. Detailed Budget

Investigators

The principal investigator and the co-investigators will all work for 15 months during the regular semesters for the entire duration of the project. The principla investigator and the co-investigators will also work for one summer. They will receive payment as per the university regulations. Two graduate students will be required for the whole duration of the project to assist with the simulator development, running the experiments (simulations) and helping in the design of the router model. Their total compensation will be (SR 8000/- per Graduate Student/Research Assistant) SR 16,000/-. Hence the wages for the investigator and graduate students are as follows:

Dr. Abdelhafid Bouhraoua (PI)	SR. 1,200/- * 11 = SR.13,200/-
Dr. Muhammad F. Mudawar (Co-I)	SR. 1,000/- * 11 = SR.11,000/-
Dr. Muhammad E. S. El-Rabaa (Co-I)	SR. 1,000/- * 11 = SR.11,000/-
Graduate Students	SR. 5,000/- * 2 = SR.10,000/-
Total:	= SR.45,200/-

Equipment, Material & Supplies and Other Expenses

Facilities available at KFUPM will be used at no charge to the project. Additional equipment needed for the project includes two Desktop PC with a CPU speed of 3 GHz (or better), a 1 GB of RAM, a 80 GB Hard-drive (or better), a Flat 19" TFT Monitor, costing SR 8,000. One PC will be used by the graduate students working on the project. The other PC is required for the investigators. Also the software package, ActiveHDL, is needed for the design and simulation of the parameterized router model at a cost of SR 13,000. This is a one time license price with no subsequent renewal cost. Other expenses for simple peripherals (such as CD writers, flash memories, hard-disks, et.), consumables such as computer disks, CDs, etc., will amount to SR 3,500/-. The purchase of literature, books, stationary, etc., will require an additional SR 2,000/-. Photocopying charges, fax, telephones, etc., will amount to SR 1,500/-. Other miscellaneous incidental expenses may amount to a maximum of SR 1,500/-. Hence the total cost of equipment, consumables and supplies is estimated to be SR 27,500/-.

A secretary will work for the entire duration of the project, hence an additional SR 2,000/- for payments to secretary will be required. The individual items of the budget are summarized in Table 3 below:

Table 3 – Summary of Budget Items

Head #	Budget Item	Allocation	Remarks
1.	**Manpower**		
	Dr. Abdelhafid Bouhraoua	13,200	
	Dr. Muhammad Mudawar	11,000	
	Dr. Muhammad El-Rabaa	11,000	
	Graduate Students	10,000	
	Sub-Total	**45,200**	
2.	**Equipment, Equipment Maintenance and Material**		
	Desktop PCs (2)	8,000	
	Aldec Active HDL Software	13,000	
	Sub-Total	19,000	
3.	**Supplies**		
	Peripherals and Consumables	3,500	
	Literature books and stationery	2,000	
	Photocopying charges, fax, phone	1,500	
	Sub-Total	7,000	
4.	**Miscellaneous**		
	Secretary	2,000	
	Miscellaneous and Incidental	1,500	
	Sub-Total	3,500	
5.	**GRAND TOTAL**	**74,700**	

11. References

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12. Resume

Dr. Abdelhafid Bouhraoua's Resume:

Academic Experience

- Teaching and Student Supervising Experience

Feb. 2005 – Present: King Fahd University of Petroleum and Minerals, COE Department
Assistant Professor,
Teaching the following courses:

- COE-200 Fundamentals of Computer Engineering
- COE-205 Computer Organization and Assembly Language
- COE-308 Computer Architecture
- COE-485 Senior Project Design

Oct. 1994 – September 1997: University Pierre & Marie Curie, Paris VI, Paris, France
Research Assistant.

- Supervised two Ms. CS final projects.
- Supervised three Bs. CS and one Bs. EE final projects.

Some of the projects:

- Automatic routing scheme generation based on interval labeling (used in interconnection networks for parallel architectures); Masters Degree in Computer Science
- NDL (Network Description Language) subset parser; Bs. Degree in Computer Science

Oct. 1993 – June 1994: University Pierre & Marie Curie, Paris VI, Paris, France
Teacher Assistant for the Master of VLSI Circuit Design Program

- Taught VLSI implementation methodology and flow through a tutorial course of implementing an AMD 2901 datapath slice-processor.
  - VHDL description and behavioral simulation
  - Logic synthesis
  - Test structure insertion
  - Test pattern generation and coverage
  - Place and route
  - Pad ring
- Taught practical digital specifications of MIPS R3000 Microprocessor and guided the students through the different methodology steps focusing on the VLSI implementation steps especially using a home grown datapath generator.

Dec. 1989-Oct. 1992: Research Ministry, Algiers, Algeria
Research Engineer. Supervised 4 Bs. CS and 10 Bs. EE students' final projects in architecture design, telecommunication and CAD software areas.
Some of the projects:

- Design of a 32x32 multiplier using Booth algorithm and Wallace tree in 1um CMOS technology.
- Design of a 8K-lines PC-based telephone switch.
- Design of a single-chip micro-controller dedicated to telecommunication applications along with its PC based development and simulation environment.
- Design of a PC based digital scope software and hardware (as a PC extension board)

- Development of a high level specification CAD environment targeted to CPU designs.

- *Research Experience*

Oct. 1994-Dec.1997: University Pierre & Marie Curie, Paris VI, Paris, France
Member of the Computer Architecture group.
Software Architect for European funded project MILE(OMI/MACRAME).
Research on Interconnection Networks:

- Design and Realization of a Simulation Environment for Performance Evaluation of Interconnections Networks**:** MILE. 30,000 lines of C-Code. Contains:
  - A graphic Editor that allows the graphic edition of networks.
  - A cycle-based Simulator using the communicating FSMs model. User-defined component libraries. The component definition is compliant with the object-oriented model. Work supported by the European Union (OMI/MACRAME).
  - Performance Evaluation of several topologies: Multistage Interconnection Networks, Hypercubes, Meshes, etc...
  - Performance evaluation of several buffering strategies for message crossbar-based switches (like ATM switches). Design of the Architecture of a Switching Circuit (16x16 crossbar). Work supported by the European Union (JESSI).
  - Definition of a new theory for the verification of deadlock/livelock-freedom for routing algorithms.
  - Design of an automatic labeling algorithm for indirect networks like Multistage Networks.

Oct. 1992-June 1993: University Pierre & Marie Curie, Paris VI, Paris, France
Masters student.
Developed a portable RAM generator for ASIC designs. The generator included the development of:

- The full software of the generator that takes care of the different generation variants and options available.
- The full design of the RAM library cells which included:
  - Schematic and behavioral
  - Validation through Spice simulations
  - Layout

Dec. 1989-Oct. 1992: Research Ministry, Algiers, Algeria
Research Engineer,
Team of four researchers. In charge of the design and implementation of a 32-bit RISC microprocessor: HRISC II. Individual charge:

- Design of the Architecture and the Micro-architecture of a RISC Microprocessor: HRISC II.
- Behavioral modeling and simulation of the micro-architecture
- Full-custom VLSI implementation of the control path of HRISC II (+100K transistors)

June-Jul. 1987: Summer Internship at the Institute of Computer Engineering INI, Algiers, Algeria.
Design of a disk cache extension card architecture and software drivers for Gespac/OS9 system.

Education

May 1998: University Pierre & Marie Curie, Paris VI, Paris, France
PhD in Computer Systems Engineering and VLSI Design (with first honors).
Thesis: "Performance Evaluation of Interconnection Networks for Parallel Architectures."

June 1993: University Pierre & Marie Curie, Paris VI, Paris, France
Masters of Science in Electrical and Computer Engineering (with distinction).
Thesis: "Design and Implementation of A Portable SRAM generator."

October 1989: Algiers Institute of Computer Science INI, Algiers, Algeria.
Bachelor of Science in Electrical Engineering and Computer Science.
Thesis : "Architecture and Micro-Architecture Design of a 32 bit RISC Microprocessor."

Technical Skills

Computer Architecture Design: Multiprocessor and Parallel Architectures, RISC, CISC (Microcontrollers), Superscalar, FPU and DSP.

Microprocessors/Microcontrollers:
- Architecture: Intel x86, Atmel Microcontrollers, ARM7, MIPS R2000/3000/4000.
- Busses: ISA, VME, PCI

VLSI Circuit Design: Complete ASIC flow mastering:

Telecommunications:
- ATM: Design of switches and SARs
- High speed Fiber: SONET/SDH, GFP (G.709)
- TDM: ST-BUS/GCI,
- Access: T1/E1/J1,T3/E3/J3, ADSL, VDSL
- LAN: Ethernet: 10/100/1000/10G protocols, MII, RMII, SMII, S3MII, GMII, MACs, PHY negociation, VLAN tagging
- Link Layer: HDLC bit and byte protocol.

Software: C, C++, Java, CORBA, ORBix, Unix, MS-Windows 95/NT+API, X11, Motif API, ITU/SDL, Telelogic SDT, TINA-C, ITU/TINA-C/ODL.

Networking: TCP/IP protocol stack and derivatives.

Industrial Experience

Oct.2001-Present: Zarlink Semiconductor, Ottawa, ON, Canada
Senior ASIC Designer and Chip Architect
Involved in several projects
- 16kx16k channels TDM switch project:
  Responsible for the verification and wrap-up design. Technical expert on the side of the RTL group dealing with the implementation group.
  - Development of the verification test suite
  - Code coverage
  - Regression and Gate level simulation
  - Timing closure
- VDSL project:
  - Responsible for the design of the Ethernet over VDSL (EoVDSL) adaptation layer block.
  - Developed a simulator to simulate the behavior of the EoVDSL layer under several conditions. Simulator developed in C. Generates industry standard waveform .vcd files.
  - Responsible for defining the architecture of a multi-channel VDSL chip.
    - Invented a new improved method to instantly compute variable packet fragment sizes to scale the fragments according to each channel data rate in order to avoid skew between fragments. A patent application has been written but has not been filed.
    - Proposed several schemes to realize the interconnection of two family of chips using either point to point parallel interfaces or point to multi-point ones in order to reduce the pin count.
- ATM AAL2 Switch:
  Responsible for the top level verification
  - Developed a high level language to describe testcases using non-deterministic methods like random number generators.
  - Merged two block level testbenches to realize the top level testbench .
  - Wrote several Perl scripts and C/PLI functions to realize the integration of the testbench component in both the block level and the top level testbenches.

June 2000-Oct. 2001: Applied Micro-Circuits Corporation, Ottawa, ON, Canada
Senior ASIC Design and Verification Engineer
Involved in several projects
- Hudson 2: OC192 (10 Gbps) G.709 Forward Error Correction Unit (Respin of Hudson 1)
  Main verification resource. Responsible for more than 40% of the verification process
  - Wrote comprehensive testcases in Perl that verify several features simultaneously
- Tiber: SRP node. Partnership with CISCO.
  Main design and verification resource
  - Designed the FIFO interface to the link layer device
  - Designed the HDLC serial port (Tx and Rx)
  - Involved in the top level integration
  - Developed a feature rich, script driven SRP packet generator
- Hudson 1: OC-192 (10Gbps) G.709 Forward Error Correction
  Participated in the verification

Nov.1999-June 2000: Cyber Technologies Corporation
Verification Engineer - Consultant on a hiring contract at Celox Networks, St Louis, MO, USA

Member of the Verification team.
Participates in the design and development of the verification toolset to perform a system level verification on a chipset which will be the core of a high performance IP intelligent router. In charge of the hardware software (verilog/C) integration. Designed and developed the following:

- verilog models that wrap up the chipset and models some board level components
- board level overall model
- library of components that communicate with the toolset via verilog PLI interface.
- verilog/C memory models to speed-up the simulation.
- Intelligent Bus snoopers
- Interface with the other modules of the toolset
- Bus functional models of POS (Packet Over SONET)

April 1998-Nov 1999: Cyber Technologies Corporation
Service Creation Environment Architect – Consultant at Sprint, Technology Planning & Integration Department, Overland Park, Kansas, USA

- Design and development of next generation service creation environment for Multi-media Multiparty Services. Project Leader. Project involves OO Design of a specialized CASE toolset dedicated to the creation of broadband multimedia services. The toolset includes:
  - GUI based service components design based on ITU-ODL (Object Description Language)
  - Integration with Telelogic SDT (ITU-SDL:Specification Description Language Tool) for Behavioral Description/Simulation/Verification.
  - Parameterizable Advanced Code(C++/Java) generation based on ODL, SDL and Service Architecture (Interactions).
  - Integration with the TINA-C DPE (Distributed Processing Environment).
- Design and Development of a Platform-Independent Service Creation Environment for narrowband services (voice mainly). Project aims to unify heterogeneous Service Creation Environments from different vendors into a unique SCE with the ability to deploy the produced service on any platform. The toolset includes:
  - GUI based component (feature) design and implementation in Java
  - Sample component library design.
  - Fully graphic Service Creation Environment featuring graphic description of the created service. Flexible tool independent from the service features. Designed and Implemented in Java.
  - Produces a service script coded in SDL.
  - Integrated with Telelogic SDT for Simulation/Verification.

Honors and Achievements

- Seymour Cray 1st Prize Laureat from CRAY Computer Company as a member of Alliance designers team, 1994 (see http://asim.lip6.fr/team/distinctions/cray94/index.fr.html)

- Best Student Paper Award, IEEE Computer Society at PDCS'96, Dijon.

Training

1998 Telelogic SDT (ITU-SDL design tool) design using SDT Toolset.

Publications

A. BOUARAOUA, A. AMARI, A. BELLAOUAR, A. AFRA & L. SAHLI, *"Micro-architecture Design of HRISC II Microprocessor"*, ICM'90, December 1990, Damas Syria.

Y.I. EL-HAFFAF, A. BOUARAOUA & A. AMARI.*"Micro-architecture Design and Implementation of HRISC II Microprocessor"*, EURO-ASIC Conference, 27th-31st May 1991, Paris France.

Y.I. EL-HAFFAF, A. BOUARAOUA & A. AMARI, *"Design and Implementation of the Data-path of a 32-bits RISC Microprocessor: HRISC II"*, EURO-ASIC Conference, 1st-5th June 1992, Paris France.

A. BOUARAOUA & A. GREINER, *"A Portable SRAM Generator"*, ICM'94, September 19th-21st 1994, Istanbul Turkey.

B. ZERROUK , A. BOUARAOUA and A. GREINER,*"Defining a New Component for the MILE simulator"*, Esprit-OMI/MACRAME Project Report, March 1995.

B. ZERROUK and A. BOUARAOUA, *"MILE Software Architecture Overview and Principles"*, Esprit-OMI/MACRAME Project Report, May 1996.

B. ZERROUK and A. BOUARAOUA, *"Evaluation of RCube Based Networks using MILE"*, Esprit-OMI/MACRAME Project Report, June 1996.

B. ZERROUK & A. BOUARAOUA, *"MILE: An Open Environment for Interconnection Networks Performance Evaluation"*, PDCS'96, September 25-27th 1996, Dijon, France.

B. ZERROUK, A. BOUARAOUA & F. ILPONSE, *"Experimental Study of a Generic Router Architecture under MILE"*, IASTED'97, February 17-20th 1997, Innsbruck, Austria.

A. BOUARAOUA, B. ZERROUK & J. FAIK, *"Adaptive Message Routing for Compact Reconfigurable Router"*, ICECS'97, December 15th-17th 1997, Cairo, Egypt.

Dr. Muhammad Mudawar's Resume:

Muhamed F. Mudawar

Assistant Professor
Computer Engineering Department
College of Computer Sciences and Engineering
King Fahd University of Petroleum and Minerals
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Last updated: November 26, 2005

1. Personal Data

Nationality: Lebanese, Born in 1963 in Beirut, Lebanon

2. Research Interests

- Processor micro-architecture
- Multiprocessors and interconnection networks
- Parallel programming environments and compilation techniques

3. Academic Degrees

Ph.D. 1993, Computer Engineering, Syracuse University. GPA 3.92 / 4.0

Area of specialization: Parallel computer architecture.
Minor: Computer and Information Science.

M.S. 1988, Computer Engineering, Syracuse University.
Area of specialization: Computer Architecture.

B.E. 1986, Electrical Engineering, The American University in Beirut. Grade: 91/100.

4. Employment History

Fall 2004 – Present : King Fahd University of Petroleum and Minerals
Fall 1993 – 2004 : American University in Cairo
Fall 1987 – 1993 : Syracuse University
Summer 1988, 1989 : Prime Computer, Framingham, MA

5. Teaching Experience

5.1 Courses Taught at KFUPM

- CSE 661: Parallel and Vector Architectures
- COE 308: Computer Architecture
- COE 205: Computer Organization and Assembly Language

5.2 Courses Taught at AUC

- CSCI 532: Parallel Computer Architecture (three times)
- CSCI 530: Contemporary Computer Design (many times)
- CSCI 491: Senior Project I (coordinator) (twice)
- CSCI 492: Senior Project II (coordinator) (twice)

- CSCI 485: Special Topics in CS - Digital Systems Design (once)
- CSCI 447: Compiler Design (many times)
- CSCI 345: Operating Systems (many times)
- CSCI 210: Data Structures and Algorithms (many times)
- CSCI 110: Programming Fundamentals (twice)
- CSCI 106: Fundamentals of Computer Science (many times)

5.3 Courses Taught at Syracuse University

- CSE 572: Switching Theory and Sequential Machine Design (three times)

5.4 Curriculum Development

- Actively participated in the development of the M.Sc. curriculum in Computer Science at AUC which led to its starting in Fall 1995.
- Actively participated in the enhancement of the undergraduate program at AUC.

5.5 Web Material for Teaching

- Developed web pages for my courses. These web pages include lecture slides, assignments, exams, lab material, course syllabi, schedules, and other related information. My teaching record can be reached at: http://www.ccse.kfupm.edu.sa/~mudawar/teaching.htm

5.6 Senior Projects at AUC

These projects are carried by groups of 3 to 5 senior graduating students and done over a period of 2 semesters. Here is a sample of the projects that I proposed and closely supervised. These projects led to successful prototypes.

- *Microprocessor Simulation and Visualization*
- *Building a Cluster from Recycled Computers*
- *Visual SIMPL (a programming language developed at AUC)*
- *A Microkernel-Based Firewall System*
- *Writing a Compiler for a Sequential Subset of SIMPL*
- *Visualizing the Internal Architecture of a Microprocessor*
- *An Experimental Virtual Machine*
- *Arabic C Programming Language*
- *Extending C with Parallel Constructs*
- *Multicode X Windows System*

6. Research

6.1 Research Projects

- (2003-2004) Introduced iterative instructions at the instruction-set architecture to exploit instruction-level and thread-level parallelism. Also, studied the effect of having parallel primary caches for instructions and data to improve the bandwidth and capacity of primary caches.

- (1999-2003) Proposed a new family of orthogonal multi-dimensional interconnection networks, called k-ary m-way networks, based on the concept of multi-way (shared) channels and two-link routers (or nodes). Wrote a simulation program to assess the performance of the newly proposed k-ary m-way network for a variety of orthogonal topologies, dimensions, routing algorithms, buffer specifications, and traffic. The simulator can produce a variety of statistics on message latency and throughput. Studied wormhole routing and broadcasting in k-ary m-way networks, and a comparative study of k-ary m-way and k-ary n-cube networks has been made. Multicasting in k-ary m-way networks is currently in progress. A router chip has been designed in VHDL.
- (1997-1998) Parallel Virtual Machines for thread distribution, scheduling and migration in a distributed environment.
- (1997-1999) Involved in the design and implementation of a new programming language called SIMPL. This language features parameterized types, polymorphic functions, the separation of interfaces from implementation, safe references, garbage collection, and higher-order functions.

6.2 Referred Publications

- Mudawar M. and Wani J., One-Level Cache Memory Design for Scalable SMT Architectures, in *Proceedings of the 17th ISCA International Conference on Parallel and Distributed Computing Systems*, September 15-17 2004, San Francisco, California, pages 290-296.
- Mudawar M., Scalable Cache Memory Design for Large-Scale SMT Architectures, *ACM International Conference Proceedings Series, Vol 68*; also in *Proceedings of the 3rd Workshop on Memory Performance Issues: in conjunction with 31st IEEE/ACM International Symposium on Computer Architecture*, June 20-23 2004, Munich, Germany, pages 65-71.
- Amer I., Badawy W., and Mudawwar M., Towards Low-Power Synthesis: A Common Subexpression Extraction Algorithm Under Delay Constraints, in *Proceedings of the 46th IEEE Midwest Symposium on Circuits and Systems*, December 27 – 30, 2003, Cairo, Egypt.
- Haddad H. and Mudawwar M., Corner-First Tree-Based Region Broadcasting in Mesh Networks, in *Proceedings of the 21st IASTED International Conference on Parallel and Distributed Computing and Networks*, February 10-13, 2003, Innsbruck, Austria, pages 615-620.
- Mudawwar M. and Saad A., The k-ary n-cube Network and its Dual: a Comparative Study, in *Proceedings of the 13th IASTED International Conference on Parallel and Distributed Computing and Systems*, August 21-24, 2001, Anaheim, California, pages 254-259.
- Mudawwar M., k-ary m-way Networks: the Dual of k-ary n-cubes, in *Proceedings of the 12th IASTED International Conference on Parallel and Distributed Computing and Systems*, November 6-9, 2000, Las Vegas, Nevada.

- Mudawwar M. and Mameesh R., Region Broadcasting in k-ary m-way Networks, in *Proceedings of the ISCA 13th International Conference on Parallel and Distributed Computing Systems*, August 8-10, 2000, Las Vegas, Nevada, pages 268-274.

- Mudawwar M., A Switch-Free Router for k-ary m-way Networks, in *Proceedings of the 2000 International Conference on Parallel and Distributed Processing Techniques and Applications*, June 26-29 2000, Las Vegas, Nevada, pages 977-983.

- Mudawwar M., Thread Programming in SIMPL, in *Proceedings of the 8th International Conference on AI Applications*, February 3-6, 2000, Cairo, Egypt, pages 373-383.

- Mudawwar M., Parameterized Types and Polymorphic Functions in SIMPL, in *Proceedings of the 8th International Conference on AI Applications*, February 3-6, 2000, Cairo, Egypt, pages 385-396.

- Mudawwar M., Multiway Channels in Interconnection Networks, in *Proceedings of the 12th ISCA International Conference on Parallel and Distributed Computing Systems*, Fort Lauderdale, Florida, August 1999, pages 506-513.

- Abdel-Radi T. and Mudawwar M., "XTPVM: Extended Threaded Parallel Virtual Machine", in *proceedings of the 11th international conference on parallel and distributed computing systems*, Chicago, Illinois, August 2-4, 1998, pages 105-112.

- Mudawwar M., "Multicode: A Truly Multilingual Approach to Text Encoding", *IEEE Computer*, April 1997, pages 37-43.

- Mudawwar M., "SIMPL: a Semi-Imperative Parallel Language", in *proceedings of the AUC Symposium on Sciences and Engineering Education*, April 1995.

- Mudawwar M. and Roger Chen C.Y., "The Signal Flow Model: A Novel Data Driven Approach to Parallel Processing", in *proceedings of the 1992 international conference on parallel processing*, August 17-21, 1992.

- Bogucz E.A. and Mudawwar M., "A Symbolic Manipulation Toolkit for Asymptotic Analysis of Viscous Flows", in *29th Aerospace Sciences Meeting*, January 7-10, 1991.

6.3 Thesis Supervision

- Ihab Mostafa Amin Amer, “Synthesis and Optimization of Digital Systems for Low Power at Logical Level of Abstraction”, Master Thesis, Computer Science Department, AUC, May 2003.

- Hadeel Youssef Samaan Haddad, “Tree-Based Regional Broadcasting in Mesh Directed Networks”, Master Thesis, Computer Science Department, AUC, December 2002.

- Aya Hassan Saad, “Associating Nodes with Routers in k-ary m-way Interconnection Networks”, Master Thesis, Computer Science Department, AUC, January 2001.

- Rania Mameesh, "Region Broadcasting in Multiway Channel Networks", Master Thesis, Computer Science Department, AUC, January 2000.

- Soha Saad Zaghloul, "Backtracking in Wormhole-Routed Interconnection Networks", Master Thesis, Computer Science Department, AUC, January 1999.

- Soumaia Ahmed Al-Ayyat, “Parametric Polymorphism in the SIMPL Language”, Master Thesis, Computer Science Department, AUC, November 1998.
- Tarek Hafez Mohammed Abdel-Radi, “XTPVM: A Transparent Thread Scheduling and Migrating Machine”, Master Thesis, Computer Science Department, AUC, April 1998.

7. Professional Activities

- Served as a member of the IASTED Technical Committee for the period 2001-2004. This Committee is responsible for the planning and the organization of IASTED activities such as conferences, meetings, and publications.
- Refereed journal papers for the Journals of Parallel and Distributed Computing and Software Practice and Experience.
- Participated in many international conferences, most of which were in the United States and Europe.
- Refereed conference papers for many conferences.
- Chaired and co-chaired sessions in various conferences.
- Active member in many professional societies, including IEEE, ACM, ISCA, IASTED, and ACM Special Interest Group on Computer Architecture (SIGARCH).

8. Services and Committees

- Initiated and supervised a project that led to the development of the Computer Science department website at the American University in Cairo.
- Active participation and chairing of some committees. These include: hardware and software committees, which are responsible of planning, purchasing, and following-up on hardware and software purchases within the Computer Science department at AUC.
- Research committee: reviewed, evaluated, and ranked research and conference applications submitted by faculty members at AUC.

Dr. Muhammad E. S. El-Rabaa Resume

Dr. Muhammad E. S. Elrabaa

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EDUCATION

B.Sc. Computer Engineering, Kuwait University, Kuwait, 1989

M.A.Sc. Electrical & Computer Engineering, University of Waterloo, CANADA, 1991

PhD Electrical & Computer Engineering, University of Waterloo, CANADA, 1995

WORK EXPERIENCE

Sept. 2001 – Present: Assistant Professor, Computer Engineering Dept., KFUPM

Taught courses and carried research in the areas of VLSI Design, Design, Simulation, and Synthesis of Digital Hardware using Hardware Description Languages, and Data Communications.

Sept. 1998 – August 2001: Assistant Professor, Electrical Eng. Dept., United Arab Emirates University, Al-Ain, UAE

Taught courses and carried research in the areas of Computers (Logic Design, Software Engineering and Design, Simulation, and Synthesis of Digital Hardware using Hardware Description Languages) and Electronics (Analog and Digital Electronics, Computer-Aided Circuit Design and VLSI). Also supervised many graduation projects in networking and communication.

Sept. 1995 – Aug. 1998: Senior Component Design Engineer, Intel Corporation, Portland, Oregon, USA

Designed, simulated, and tested digital circuits, analog circuits, and mixed digital-analog circuits. This involved working in a team as well as supervising others.

Sept. 1989 - Sept. 1995: Research Assistant, VLSI Research Group, University of Waterloo, Waterloo, Ontario, CANADA

Conducted research on digital BiCMOS, data communication, and Memory circuits. This included the design, simulations, and testing of a large variety of circuits.

May 1990 - Dec. 1994: Teaching Assistant, University of Waterloo

Worked as a teaching assistant for Electronics, Digital Logic design, and Integrated Circuit Design courses.

Jan. 1992 - Dec. 1994: **A contracted Researcher, The Microelectronics Center, NorTel Ltd., Ottawa, CANADA**

Designed, simulated, and tested a variety of high-speed communication circuits.

May 1992-Apr. 1993: A contracted Circuit Designer, Canadian Microelectronics Corporation (CMC), CANADA

Designed, simulated and developed a library of digital standard cell circuits.

May 1989 - Sept. 1989: Research Assistant, Kuwait University, Kuwait

Developed complex data structures for software that simulated neural networks.

Jan. 1989 - May 1989: Teaching Assistant, Kuwait University, Kuwait

As a senior undergraduate student worked as a teaching assistant for a 4th year computer operating systems course

ACCOMPLISHMENTS AND HONOURS

- Was awarded two US patents
- Received three research grants as an assistant professor in UAE University; two as a primary investigator and one as a co-investigator totaling over SR 300,000
- Reviewed many papers for international journals and conferences
- Gave many tutorials in workshops and conferences
- Attended many workshops and international conferences
- Supervised many undergraduate senior design projects

- Was awarded many scholarships in the University of Waterloo during my graduate study
- Was placed on the dean's list during all my undergraduate study

List of Publications

a) Patents

1. M. S. Elrabaa and M. I. Elmasry, "Low-Power BiCMOS/ECL SRAM" United States Patent # 5,602,774, awarded in Feb. 11th, 1997.
2. M. S. Elrabaa, M. I. Elmasry, and D. S. Malhi, "A BiCMOS Transceiver (Driver and Receiver) for Gigahertz Operation" United States Patent # 5,966,032, awarded in Oct. 12th, 1999.

b) Books

1. Muhammad E. S. Elrabaa, I. S. Abu-Khater, and M. I. Elmasry, "Advanced Low-Power Digital Circuit Techniques" Kluwer Academic Publications, USA, 1997.

c) Journal Papers

1. Muhammad E. S. Elrabaa, "An All-Digital Clock Recovery and Data Retiming Circuitry for High Speed NRZ Data Communications," Institute of Electronics, Information and Communication Engineers (Japan) Transactions on Electronics, Vol. E85-C, No. 5, P. 1170, May, 2002.
2. Muhammad E. S. Elrabaa, Mohab Anis, and Mohamed Elmasry, "A Contention-Free DOMINO Logic For Scaled-Down CMOS," Institute of Electronics, Information and Communication Engineers (Japan) Transactions on Electronics, TVol. E85-C, No. 5, P. 1177, May, 2002.
3. Muhammad E. S. Elrabaa, M. I. Elmasry, and D. S. Malhi, "Low-Power BiCMOS Circuits for High-Speed Interchip Communication," IEEE Journal of Solid-State Circuits, vol. 32, PP. 604-609, April 1997.
4. Muhammad E. S. Elrabaa, M. Obrecht, and M. I. Elmasry, "Novel Low-power Low-voltage Full Swing BiCMOS Circuits," IEEE Journal of solid-state Circuits, vol. 29, PP. 86-94, Feb 1994.
5. Muhammad E. S. Elrabaa and M. I. Elmasry, "Design and Optimization of Buffer Chains and Logic Circuits in a BiCMOS Environment," IEEE Journal of solid-state Circuits, vol. 27, PP. 792-801, May 1992.
6. Muhammad E. S. Elrabaa and M. I. Elmasry, "Multi-Emitter BiCMOS CML Circuits," IEEE Journal of solid-state Circuits, vol. 27, PP. 454-458, March 1992.

d) Conference Papers

1. Muhammad E. S. Elrabaa, “REVIEW OF HIGH-SPEED DIGITAL CMOS CIRCUITS,” *To Appear in the 6th Saudi Engineering Conference*, Dhahran, Dec. 2003.
2. Muhammad E. S. Elrabaa and M. I. Elmasry, “Split-Gate Logic Circuits for Multi-Threshold Technologies,” International Symp. On Cir. And Systems (ISCAS’01), Sydney, Australia.
3. Muhammad E. S. Elrabaa, M. I. Elmasry, and D. S. Malhi, "A Universal 3.3V 1GHz BiCMOS Transceiver (Driver/Receiver," Proc. of the IEEE Bipolar /BiCMOS Circ. and Tech. Meeting, PP. 118-120, Minnesota, 1995.
4. Muhammad E. S. Elrabaa and M. I. Elmasry, "Low-Power Circuit Techniques for High-Speed ECL SRAMs," Proc. of the 21st European Solid-State Circuits Conference (ESSCIRC), France, 1995.
5. Muhammad E. S. Elrabaa and M. I. Elmasry, "Optimization of Digital BiCMOS Circuits, An Overview," An Invited Tutorial, Proc. of the 35th Midwest Symp. On Circuits and Systems, pp. 571-574, 1992.

Seminars Attended:

1. **Gave a seminar titled “Design of Digital BiCMOS Logic Gates,” in the 1992 CMC (Canadian Microelectronics Corp.) VLSI Workshop in Kingston Ontario.**
2. Gave a seminar titled “Design of Digital BiCMOS and ECL Standard Cell Liberary for CADENCE Design Environment,” in the 1993 CMC (Canadian Microelectronics Corp.) VLSI Workshop in Kingston Ontario.
3. Gave a seminar titled “Design of Full-Swing BiCMOS Buffers,” in the 1994 ITRC (Ontario Center of Excellence Annual Meeting)
4. Attended Several conferences (Bipolar Cir. And Tech. Meeting (BCTM) 1990, Int. Electron Devices Meeting 1991, ASIC Conference 1993, Medwest Symp. 1993, BCTM 1995, Int. Solid-State Cir. Conf. (ISSCC) 1997)