# King Fahd University of Petroleum and Minerals College of Computer Science and Engineering COMPUTER ENGINEERING DEPARTMENT 

## COE 202-Term 053 <br> Assignment \#4

## Q. 1 (20 points)

A designer desires to design a combinational circuit that inserts a 0 in a given bit in an 8 -bits number A (A7 to A0). A7 is the MSB and A0 is the LSB

1. Give the circuit that realizes the function described above using decoders.
2. Give the circuit that realizes the function described above using multiplexers

## Q. 2 (30 points)

A circuit designer needs a block of combinational logic that has the following specifications:

- 3 inputs A, B and C
- 1 enable input En
- 8 outputs Y7 to Y0

The block truth table is given below:

| En | $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{C}$ | $\mathbf{Y 7}$ | $\mathbf{Y 6}$ | $\mathbf{Y 5}$ | $\mathbf{Y 4}$ | $\mathbf{Y 3}$ | $\mathbf{Y 2}$ | $\mathbf{Y 1}$ | $\mathbf{Y 0}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

1. Design a circuit that uses decoders and gates to realize the function represented in the truth table. The number of decoders and gates should be minimum.
2. Consider the following curcuit:


The truth Table associated with it is given below:

| Din | All | S | K1 | K0 |
| :---: | :---: | :---: | :---: | :---: |
| 0 | X | X | 0 | 0 |
| 1 | 1 | X | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |

Find the simplified equations of this circuit.
3. Build the circuit of 1 . using the circuit of 2 . as a building block. Do not show the gates that make the circuit in 2 . Use only the block diagram as shown in the figure above.
4. Which solution between 1 and 3 is more advantageous? Justify your answer.

## Q. 3 (20 points)

A 4 to 2 priority encoder has:

- 4 inputs labeled A3 to A0
- 3 outputs labeled Y1 and Y0 for the encoded value and a VALID output used to indicate whether the encoded value is valid or not. The VALID signal, as explained in the lecture, is used to make the difference between when no input is active and when A0 is active as in both cases, the outputs Y1 and Y0 are equal to 00 .

1. Using only 4 to 2 priority encoders and 2 to 1 multiplexers realize an 8 to 3 priority encoder.
2. Using only 4 to 2 priority encoders and 2 to 1 multiplexers realize a 16 to 4 priority encoder.
3. Using only 4 to 2 priority encoders and 2 to 1 multiplexers realize a 10 to 4 priority encoder which outputs a 4-bits BCD digit.

## Q. 4 (20 points)

Consider a 2 to 1 multiplexer that has two inputs D 1 and D 0 , a selection input S and an output Y . The output $Y$ is inverted. So, when $\mathrm{S}=0$, Y will select D 0 inverted which means $\mathrm{Y}=\mathrm{D} 0$ '. When $\mathrm{S}=1, \mathrm{Y}=\mathrm{D} 1$ '.

1. Show the connections to one 2-to-1 multiplexer that make it realize an inverter of an input $A$.
2. Show the connections to one 2-to-1 multiplexer that make it realize an AND gate of two inputs A and B.
3. Show the connections to one 2-to-1 multiplexer that make it realize an OR gate of two inputs $A$ and $B$.
4. Show the connections to one 2-to-1 multiplexer that make it realize a XOR gate of two inputs $A$ and $B$.
5. Show the connections to one 2-to-1 multiplexer that make it realize a XNOR gate of two inputs A and B.
Except for 1., allowed connections are:

- Inverted variable (A' or B')
- Logic ' 1 '
- Logic '0’

