Flip-Flops

Cross-NOR SR flip-flop

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Cross-NAND SR flip-flop

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Q</td>
<td>Q</td>
</tr>
</tbody>
</table>
Clocked Level-Triggered NAND SR Flip-Flop

<table>
<thead>
<tr>
<th>CLK</th>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>(\overline{Q})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>(\overline{Q}) hold</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Q</td>
<td>(\overline{Q}) hold SR inputs</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Q</td>
<td>(\overline{Q}) hold disabled</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Q</td>
<td>(\overline{Q}) hold</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>(\overline{Q}) hold</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>(\overline{Q}) reset SR inputs</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>(\overline{Q}) set enabled</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Q</td>
<td>(\overline{Q}) indeterminate</td>
</tr>
</tbody>
</table>
We can make the level triggered flip-flop more flexible (in terms of timing control) by turning it into an edge-triggered flip-flop. An edge-triggered flip-flop only samples the inputs during either a positive or negative clock edge. This conversion can be done by taking the clock signal and running it through a level-triggered, pulse generator network and taking the corresponding output as the clock signal.
Level and Edge Triggered Flip-Flop Symbols

- no triangle means level-triggered
- triangle means edge-triggered
- inverted output (complement)
- no bubbles means active-HIGH input
- bubble next to triangle means negative edge-triggered input

no bubble next to triangle means positive edge-triggered input
D-Type Flip-Flops

Basic D-type flip-flop or latch

D (data)

NAND made into an inverter

<table>
<thead>
<tr>
<th>D</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Set

Reset

logic symbol
At clock pulse edge, \( Q \) goes to \( D \).

So every time there is a clock pulse, \( Q \) is set to the old value of \( D \). Therefore, \( \overline{Q} \) changes (as does \( D \)) but by the time \( D \) changes, the edge is past.
Stop-Go Indicator

D  Q
Q
300Ω

D  Q
Q  green
red

LED
300Ω
Divide-by-Two Counter

\[ D = Q \]

\[ Q \]
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Synchronizer
We see timing is important, so we want to synchronize signals.

Synchronizer 2

Lined up with clock, but not result of pulse.
JK Flip-Flops

Clock (C) → pulse generator

J → positive edge-trigger
K → negative edge-trigger

Positive edge-trigger:

<table>
<thead>
<tr>
<th>J</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>Q</td>
</tr>
</tbody>
</table>

Negative edge-trigger:

<table>
<thead>
<tr>
<th>J</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td></td>
</tr>
<tr>
<td>K</td>
<td>Q</td>
</tr>
</tbody>
</table>
The problem is that you can not “hold” this condition. The input 1,1 can only hold outputs of (0,1) or (1,0).
JK Flip-Flops 3

Positive edge-trigger

<table>
<thead>
<tr>
<th>C</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>↓</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>↑</td>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>↑</td>
<td>1</td>
<td>1</td>
<td>Q</td>
<td>Q</td>
</tr>
</tbody>
</table>

Negative edge-trigger

<table>
<thead>
<tr>
<th>C</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>↑</td>
<td>X</td>
<td>X</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>↓</td>
<td>0</td>
<td>0</td>
<td>Q</td>
<td>Q</td>
</tr>
<tr>
<td>↓</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>↓</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>↓</td>
<td>1</td>
<td>1</td>
<td>Q</td>
<td>Q</td>
</tr>
</tbody>
</table>
JK Flip-Flop with Preset and Clear

Q
PRE
K
CLR
CLK

Q̅
JK Flip-Flop with Preset and Clear
(Negative Edge-Triggered)

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>$\overline{Q}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↓</td>
<td>0</td>
<td>0</td>
<td>$Q_0$</td>
<td>$\overline{Q}_0$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↓</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↓</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>0,1</td>
<td>1</td>
<td>$Q_0$</td>
<td>$\overline{Q}_0$</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↓</td>
<td>1</td>
<td>1</td>
<td>$\overline{Q}_0$</td>
<td>$Q_0$</td>
</tr>
</tbody>
</table>

$Q_0 = \text{state of } Q \text{ before HIGH-to-LOW edge of clock.}$
JK Flip-Flop with Preset and Clear
(Positive Edge-Triggered)

<table>
<thead>
<tr>
<th>PRE</th>
<th>CLR</th>
<th>CLK</th>
<th>J</th>
<th>K</th>
<th>Q</th>
<th>Q̅</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>0</td>
<td>0</td>
<td>Q₀</td>
<td>Q₀̅</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>1</td>
<td>0</td>
<td>Q₀</td>
<td>Q₀̅</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↓</td>
<td>0,1</td>
<td>1</td>
<td>1</td>
<td>Q₀</td>
</tr>
</tbody>
</table>

Q₀ = state of Q before LOW-to-HIGH edge of clock.
MOD-16 Ripple Counter/divide-by-2,4,8,16 Counter

+5V

CLK

CLR

divide-by-2  divide-by-4  divide-by-8  divide-by-16

Q0  Q1  Q2  Q3

CLK

CLR

Q0  Q1  Q2  Q3

Q0  Q1  Q2  Q3

Q0  Q1  Q2  Q3

0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

6.071 Digital Logic

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This circuit will count up to 15 and then disable (all bits = 0). Note: If one uses the $Q's$ as the counting bits instead of the $Q'$s, the Counter will count down from 15 and disable when 0 is reached.
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MOD-16 Synchronous Counter

+5V

CLK

CLR

divide-by-2

divide-by-4

divide-by-8

divide-by-16

Q0

Q1

Q2

Q3

0000

0001

0010

0011

0100

0101

0110

0111

1000

1001

1010

1011

1100

1101

1110

1111

0000

0001

0010

0011

0100

0101

0110

0111

1000

1001

1010

1011

1100

1101

1110

1111

0000
The 7493’s internal structure consists of four JK flip-flops connected to provide separate MOD-2 and MOD-8 sections. Both of these are clocked by separate clock inputs. The MOD-2 uses \( C_{p0} \) as its clock input while MOD-8 uses \( C_{p1} \).

### 4-Bit Counter IC

<table>
<thead>
<tr>
<th>MR₁</th>
<th>MR₂</th>
<th>( Q_0 )</th>
<th>( Q_1 )</th>
<th>( Q_2 )</th>
<th>( Q_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>count</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>count</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>count</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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### 74193 Presettable 4-bit Binary Up/Down Counter

**Inputs**
- MR
- PL
- CpU
- CpD
- D0
- D1
- D2
- D3

**Outputs**
- Q0
- Q1
- Q2
- Q3
- TCU
- TCD

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR, PL, CpU, CpD, D0, D1, D2, D3</td>
<td>Q0, Q1, Q2, Q3, TCU, TCD</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mode</th>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset</td>
<td>H X X L X X X X</td>
<td>L L L L H L</td>
</tr>
<tr>
<td></td>
<td>H X X H X X X X</td>
<td>L L L L H H</td>
</tr>
<tr>
<td>Parallel load</td>
<td>L L L X L L L L</td>
<td>L L L L H L</td>
</tr>
<tr>
<td></td>
<td>L L L X H H H H</td>
<td>L L L L H H</td>
</tr>
<tr>
<td></td>
<td>L L H X H H H H</td>
<td>H H H H L H</td>
</tr>
<tr>
<td></td>
<td>H L H H L L L L</td>
<td>H H H H H H</td>
</tr>
<tr>
<td>Count up</td>
<td>H H ↑ H X X X X</td>
<td>Count up H H</td>
</tr>
<tr>
<td>Count down</td>
<td>L H H ↑ X X X X</td>
<td>Count down H H</td>
</tr>
</tbody>
</table>

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH voltage transition
Serial in / Serial out:

Serial in: \( \ldots 0 \, 1 \, 0 \)

Serial out: \( 0 \, 0 \, 1 \ldots \)

Parallel in / Serial out:

Parallel in: \( 1 \, 0 \, 1 \, 1 \, 0 \, 1 \, 0 \)

Serial out: \( 0 \, 0 \, 1 \ldots \)

Serial in / Parallel out:

Serial in: \( \ldots 0 \, 1 \, 0 \)

Parallel out: \( 1 \, 0 \, 1 \, 1 \, 0 \, 1 \, 0 \)

Parallel in: \( 1 \, 0 \, 1 \, 1 \, 0 \, 1 \, 0 \)
Some device creating power -
There are two modes for destruction
1.) Short term $t_{on}$ is too long. Instantaneous heat load too high. Assume no heat dissipation during $t_{on}$.
2.) Long term - duty cycle $t_{on}/t_{off}$ too high.
∴ Test for 2 conditions
$t_{on} < t_{max}$
$t_{on}/t_{off} <$ duty cycle

ON

clock/n

≡

period

up
down
reset

If overflow trigger relay
$2^n = t_{max}$
If zero disable, clock until next ↑ edge of ON

n-bits

MSB
LSB

counter
zero?

6.071 Digital Logic
Problem

Explain why mon-stable is not so useful.

Solve problem using:

1x 555 - clock
flip/flops, simple logic …
1x up/down counter
borrow
carry
clear
4-bit Serial in/Serial out Shift Registers

Serial in
… 0 1 0 → Shift Right → Serial out
1 0 1 1

Serial out
… 0 0 1 → Shift Left → Serial in
1 1 0 1

Serial Input

Serial Output

D0 Q0
CLK
ff 0

D1 Q1
CLK
ff 0

D2 Q2
CLK
ff 0

D3 Q3
CLK
ff 1

Serial Input

Serial Output

D3 Q3
CLK
ff 0

D2 Q2
CLK
ff 0

D1 Q1
CLK
ff 0

D0 Q0
CLK
ff 0

Serial Input

Serial Output

D3 Q3
CLK
ff 2

D2 Q2
CLK
ff 2

D1 Q1
CLK
ff 2

D0 Q0
CLK
ff 2

Clock

Serial Input

Serial Output

Clock
Parallel-to-Serial Shift Register

The diagram shows a parallel-to-serial shift register with the following inputs and outputs:

- **D0, D1, D2, D3**: Parallel inputs
- **Q0, Q1, Q2, Q3**: Shifted serial output
- **CLK**: Clock input
- **SHIFT/LOAD**: Control signal for shifting or loading data
- **Serial Output**: Output of the serial data
- **Inhibit**: Control signal to inhibit the shift

The timing diagram illustrates the clocking and shifting process, showing how data is shifted through the register with each clock pulse.
8-Bit Serial-to-Parallel Data Converter

- **+5V**
- **Vcc**
- **MR**
- **DSb**
- **DSa**
- **CLK**
- **GND**
- **Q0**
- **Q1**
- **Q2**
- **Q3**
- **Q4**
- **Q5**
- **Q6**
- **Q7**
- **D0**
- **D1**
- **D2**
- **D3**
- **D4**
- **D5**
- **D6**
- **D7**

**Inputs:**
- Serial data input
- Clock

**Outputs:**
- 8-bit Parallel word

**Other Components:**
- Octal D-type Flip-flop
- Divide-by-8 counter
8-Bit Parallel-to-Serial Interface

- Parallel in
- ASCII "&"
- Parallel load
- Clock enable
- LSB comes out first

<table>
<thead>
<tr>
<th>D0</th>
<th>D1</th>
<th>D2</th>
<th>D3</th>
<th>D4</th>
<th>D5</th>
<th>D6</th>
<th>D7</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

- PL
- CE
- CLK

Output: 00100110

Serial Device

VCC +5V

GND 0 1 2 3 4 5 6 7

Q7 Q6 Q5 Q4 Q3 Q2 Q1 Q0