Heterostructure Bipolar Transistors : From Devices to Products

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Abstract

The bottleneck for the development of high capacity fiber communication system is mainly the electronic modules due to the low speed of the used transistors. The fiber capacity is close to 1Tbits/s while the electronic circuits can currently handle a maximum of 10-40 Gb/s. The high speed of the HBTs, whether based on III-V or SiGe materials, is known. However, the technology of HBTs is in general still developing with many commercial products started to appear in early 1990s. HBTs are increasingly used in communications systems especially in transmitters/receivers. InP HBTs are known for their higher speed but are not as developed as GaAs HBTs, while SiGe devices have the advantage of their compatibility with Si. The thermal management of power HBT is being resolved. The cost of making HBT circuits is high. This paper will present a review of the above issues and includes a design of an HBT, its fabrication and characterization. It will discuss the manufacturability and reliability testing. Some of the current products and future applications of HBTs will be presented.

1. Introduction

The need to transfer and process 10-40Gb/s optical signal in communication system and the required 1-100GHz analog and digital circuits have allowed the development of high frequency products based on HBTs [1-4]. In the following sections, the design, fabrication and the characteristics of an InP HBTs, and a manufacturable GaAs HBT process will be briefly presented. A reliability evaluation process of HBT and its thermal management will be reviewed. Some of current HBT products and future applications will be listed

2. HBT design and fabrication

2.1 Design of HBTs

The Si BJT performance at microwave frequency is very poor due to mainly the high resistance of the base (B) layer, the absence of an insulating Si substrate, and low mobility of electrons in Si. The use of a heterojunction at the base-emitter BE junction allows an increase in the base doping up to $10^{20}cm^{-3}$ base (to lower the base resistance r_b) while maintaining a good current gain β as shown below for an npn transistor:

$$\beta=[(D_{nB}N_EL_{pE})/(D_{pE}N_Bw_B)]e^{\Delta E_V/kT} \quad (1)$$

where ΔE_V is the valence band discontinuity of the emitter (E) and base (B) materials (ΔE_V =0 for Si BJT), D_{nB} and D_{pE} are the diffusion constants of electrons and holes in the (B) and (E) , w_B is the (B) thickness, L_{pE} is the hole diffusion length in (E), N_E and P_B are the doping densities of (E) and (B). It is desirable to have a large ΔE_V to increase the barrier to the back-injection of holes from the (B) into the (E). Table 1 gives the values of Conduction and Valence Bands discontinuities ΔE_C and ΔE_V of various HBT Emitter-Base structures.

Table 1 : ΔE_C and ΔE_V of EB Junctions [2,7]

Emitter /Base	Si/ Si 0% Ge	InP/ InGaAs 47% Ga	InGaP /GaAs 50% In	AlGaAs /GaAs 30% Al	Si/ SiGe 20% Ge
ΔE_C	0	.25 eV	.2 eV	.25eV	~0
ΔE_V	0	.35 eV	.3eV	.13eV	.15eV
E_g/E_g (eV)	1.12/ 1.12	1.35/ 0.75	1.92/ 1.42	1.79/ 1.42	1.12/ 0.97

HBT structure is similar to that of BJT but the EB is not a homojunction. The material of the (B) and (E) is chosen based on system requirements, table 2 gives few properties of some used semiconductors. The quality of epilayers growth partly defines the device performance. The HBT emitter sizes must be reduced to minimize current crowding around the emitter periphery; however, little improvement are seen for emitter width below 1-2μm due to the large collector-base parasitic capacitance [8].

Table 2 : Some of the properties of currently used semiconductors in HBTs [2,9,10]

material	Si	GaAs	InP	$Si_{0.8}Ge_{0.2}$
E_g (eV)	1.12	1.42	1.35	.97
typical f_T f_{max} (GHz)	~25, 40	~114, 148	~140, 220	~75, 65
cost	Low	high	high	low/med
Reliability	good	good	poor	good

HBT V_{be}	low	high	low	low

The BE heterojunction is very critical to the performance of the HBT. The (B) material can be SiGe, GaAs, or InP materials and it is a lower bandgap semiconductor than the (E)'s, but has the same lattice constant. The collector (C) material and thickness affects the breakdown voltage BV_{cbo} [11] which, for power devices, must be high with no speed compromise. This requires the collector semiconductor to have a large bandgap. The layer structures of a Double HBT (both the BE and the BC are heterojunctions) is given as :

Table 3 : Epi-structures of npn InP/$In_{.47}Ga_{.53}As$ /InGa As P DHBT grown by MOCVD. [11]

Layer	Material	Thick	Doping	Density
E-cap	InGaAs	150nm	n(S)	$1x10^{19}cm^{-3}$
Emitter	InP	50nm	n(S)	$1x10^{19}cm^{-3}$
Emitter	InP	100nm	n(S)	$1x10^{18}cm^{-3}$
base	InGaAs	10nm	undoped	----------
base	InGaAs	50nm	p(Zn)	$1.5x10^{19}cm^{-3}$
collector	InGaAs	90nm	undoped	$10^{16}cm^{-3}$ (p)
collector	InGaAsP*	300nm	undoped	$10^{16}cm^{-3}$ (p)
etch-stop	InP	10nm	n(S)	$1x10^{19}cm^{-3}$
sub.col.	InGaAs	400nm	n(S)	$2x10^{19}cm^{-3}$
buffer	InP	300nm	undoped	----------
substrate	InP	500um	SI (Fe)	

* The energy gap of the used InGaAsP is 1.13eV

The EB pn junction must occurs exactly at the EB heterointerface otherwise the device performance is affected. This is the reason for the use of a 10nm undoped Base spacer layer. The base thickness should be very thin to increase the speed of the device response but not at the price of high base resistance r_b. This requires to have a high (B) doping. The reduction of the CB capacitance C_{bc} and of r_b is critical for high frequency performance, this can be done by careful layer structure design and suitable fabrication steps.

2.2 Fabrication of InP/InGaAs HBTs

Self-aligned emitter to the base is important to reduce r_b. The passivation of the base surface is critical for GaAs-based HBTs due to the high surface recombination of GaAs compared to InGaAs or SiGe. The best passivation is to leave a thin but depleted emitter layer on the base, this reduces the base leakage current at low V_{be}. Decreasing the BC capacitance may be achieved by ion implantation of the extrinsic (C) or etching it.
The main fabrication steps of the InP HBT are :
Cleaning of the wafer in Hot solvents (Tricho, Metahnol, and IPA at 80C, and Acetone). Resist is patterned to define the emitter, Wet etching of InGaAs then InP emitter layer selectively (it stops at the InGaAs (B) material), removal of resist in Acetone. The above steps are repeated to wet etch the base layer. The quaternary collector is dry etched. Similarly, the sub-collector layer is wet etched (device isolation). A resist pattern is defined with an overhang edge to be able to do the lift-off of the evaporated ohmic metal (NiGeAu for the emitter and collector, and TiPtAu for the base). Rapid thermal annealing of evaporated p and n-ohmic contacts is performed at a Temperature of 380C for 30 seconds. A SiN thin film is sputtered on the wafer, via holes in SiN are etched. Thick TiAu is deposited to define the probing pads for the HBT. The total number of mask levels to fabricate a high frequency HBT is 7 : (E)layer etch; (B) and (C) layer etch; isolation etch; (E) and (C) metals; (B) metal; Via holes; Metal pads. A cross section of the HBT (before metallisation) is shown below :

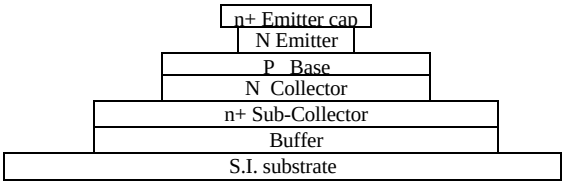

Fig. 1 : Cross section of HBT after etching the (E), (B) and (C) layers, before Ohmic metals deposition

2.3 Characteristics of the fabricated HBT

Emitter sizes were 3x5 (high frequency HBT) to 90x90 μm^2. The best HBT had an emitter size of $6x4\mu m^2$. The I-V and Gummel plots of the fabricated InP HBT [11] reflects a β>8 for over 9 orders of magnitude of I_c, BV_{cbo} > 10V, the based and collector ideality factors of n_c=1.04 and n_b=1.08. The high frequency response of the InP device were measured using HP8510 network analyzer, at the frequency range of 0.5-42 GHz, by measuring the [S] parameters. The current gain [h] and the unilateral power gain [U] are computed from [S]. f_T and f_{max} are the frequencies at which [h] and [U] are unity respectively, they had maximum values of 54, 20 GHz at I_c=30mA for a similar size (E) HBT but with InGaAs collector.

3. Reliability of HBTs

A device is reliable if its performance changes within allowed limits under specific conditions for a specific time. The failure mechanism must be defined as a drift of one of the characteristics of the device (gain, V_{be}, BV_{bco}, f_T, f_{max}, ...) by a certain percentage (15% or 30%). The next step is to understand the causes of the early failures using SEM, Optical microscope and other necessary tools, then look for ways to solve the problem. Some of the failure mechanism of HBTs are :

Hydrogen effect on Carbon-doped HBTs, the out diffusion of Base dopants into the emitter (Zn and Be in III-V, (B) in SiGe [2]), this will reduce the gain at low currents density, a way to solve it is to use C dopants or reduce the (B) doping and use a thicker undoped base spacer layer at the (E) side.

A device may be used in a product if its lifetime exceeds the minimum requirements set by the customer. This lifetime is usually extrapolated from the reliability experiments of the device under test. High temperature stress testing is done to the whole device under normal operating conditions (mainly DC biasing only and/or with RF input signals). This speeds up the failure mechanism to allow a quick study of the robustness of the HBT; however, these experiments usually take from one to three months and are relatively lengthy. The chosen stress temperatures of the oven are critical and range between 180C-250C, the low T-limit sets the length of the experiment and also its precision, the high-T limit is set usually by the sudden and catastrophic failures of some of the materials used to make the HBT due to the too high oven T. To extrapolate the lifetime of a device, we assume that the rate R of occurrence of failure is given by the Arrhenius equation :

$$R=R_o\exp(-E_a/kT) \qquad (2)$$

R_o is a constant, E_a is the activation energy, k is the Boltzman's constant, T is the absolute temperature. if we replace R=1/t (failure happens linearly with time and at a constant temperature, the above equation becomes :

$$\ln(t)=A + E_a /kT \qquad (3)$$

where A is a constant. The lifetime t_L of the device at the operating temperature T_L is given by the above equation if the constant A and the activation energy E_a is determined. This can be achieved experimentally by accelerating the failure of the device at two, preferably three, high temperatures (put say 6 devices in each of the three ovens whose temperatures are T_1=500K, T_2=530, T_3=550K), then record the time (t_1, t_2, t_3) at which 50% of the devices fail for each oven. Then equation (3) can be plot and E_a and the lifetime can be extracted.

Each failure (defect) is characterized by an activation energy E_a which is typically larger than 1.6eV for reliable devices. The highest E_a reported was 2.0eV (it corresponds to a lifetime of 10^6h at a junction T of 200C) [28]. Products based on HBTs are in the market, they show a lifetime (MTTF) of more than 10^8 hours at an operating T of 125 C.

4. Comparison of HBTs, FETs, and Si devices (based on system requirements).

Table 4 : Comparison between III-V HBTs and FETs, Si/Ge and Si devices [1,2,12-14]

Devices	III-V HBT	III-V FET	Si/SiGe	Si
noise	low	lowest	low	low
linearity	highest	med/high		low
efficiency	highest	high		low
BV_{bco}	high	med/high	low	low
speed	high	high	med.	low
power density	highest	low	high	high
reliability	high	low/high		high
cost	high	medium	low	low
$fT.BV_{bco}$	>800GHz.V		450	360
Lithography	2μm	0.25μm	0.35μm	0.25
chip size	smallest			
wafer size	3"-4" -6"	3"-4"-6"	8"-12"	8-12"

There is a competition between HBTs, GaAs FETs, and Si devices depending on the system requirements. Table 4 gives the details of the comparison between HBTs, FETs and Si devices. HEMT (High Electron Mobility Transistor) is extensively used in low noise preamplifiers but suffers from shortlifetime if used as a power device. GaAs MESFET dominates the PCS (Personal Communication System) market (0.9,2 GHz) along with Si devices. InP HBTs are the best candidate for 40GB/s optical communication system in addition to their compatibility with the monolithic integration of InP optical devices [5].

5. Manufacturability of HBTs

A fabrication process is considered manufacturable when it has the following properties : Reproducible with good control of its device characteristics (Current gain, V_{be}, BV_{bco}, f_T, f_{max}, Base sheet resistance, Ohmic contact resitances, resistivity of thin film resistors, via-holes, quality of sputtered dielectric....), good yield, acceptable cost of the chip (the wafer size and its cost, process, assembly-handling-interfacing, testing and packaging ....), good control of the growth of the epilayers of the HBTs (doping levels, layer thickness, pn heterojunction), Reliable devices, availability of high quality passive elements (R, L, C) for rf and microwave applications. A brief manufacturable process of GaAs HBT from NORTEL [17] is presented next.

Table 5 : Epi-structures of npn manufacturable graded GaAlAs/GaAs SHBT grown by CBE [17]

Layer	% Al	Thick	Doping	Density
E-cap	0	200nm	n(Si)	$5x10^{18}cm^{-3}$
Emitter	30-0	20nm	n(Si)	$5x10^{17}cm^{-3}$
Emitter	30	30nm	n(Si)	$5x10^{17}cm^{-3}$
Emitter	5-30	15nm	n(Si)	$5x10^{17}cm^{-3}$

base	0-5	60nm	p(C)	$5x10^{19}cm^{-3}$
collector	0	350nm	n(Si)	$5x10^{16}cm^{-3}$
sub.col.	0	350nm	n(Si)	$4x10^{18}cm^{-3}$

The most important fabrication steps are : He implantation for isolation and to reduce C_{bc}, dummy Si_3N_4 emitter formation, dry etch to AlGaAs emitter and p-ohmic base metal formation (self-aligned), emitter dielectric side wall formation, dry etch to sub-collector, removal of dummy emitter and n-ohmic metal deposition, (E) and (C) contacts. Then the back end process which consist mainly of : SiON deposition and via etch, NiCr resistors deposition, me1 deposition, me1 to me2 post metal deposition, BCB planarization and me2 deposition, then final dielectric deposition. The GaAs base is passivated with the nonetch of a thin depleted AlGaAs. The f_T and f_{max} exceeded 80 GHz. Recently [18] AlGaAs emitter was replaced with InGaP for uniformity and reliability improvements, higher ΔE_V the absence of DX centers, and the improved selective etching . Such HBTs are currently used in OC192 communication systems [18]. Similarly SiGe HBT technology was established and is ready for production since 1993 at IBM [2,6], it uses the very well mature Si technology line processing (easy integration with the well developed BJT/MOS technology resulting in a lower cost than III-V HBTs).

6. Thermal management and Packaging of HBTs

This is considered as a top development priority for HBT RF power amplifier. The operating temperature, known also as the junction Temperature T_j, should be as small as possible to achieve the expected performance during the lifetime of the HBT-based circuit. T_j is mostly in the range of 80C to 130C due to HBT heat dissipation which can be high for low efficient device (efficiency is around 40% to 70%) and/or the use of large signal in amplifiers. The device cooling is important and heat should be conducted away from the junctions of the device to insure proper operation and good reliability. GaAs substrate is a poor conductor compared to Si (Thermal conductivity of Si, InGaAs, GaAs, and InP are 1.31, 0.05, 0.46, and 0.74 W/cm-K respectively). This problem was elevated by thinning the GaAs substrate to 50-100µm to reduce the heat path and consequently the thermal resistance. This substrate thinning, followed by via holes making and backside thick metallisation, is a standard in making GaAs power amplifiers, eventhough it reduces the yield due to wafer breakage. The second approach is the use of thick metal thermal shunt on the emitter and a thermal metal spreader to take heat from the top of the device and back to the GaAs surface. The third approach that is more promising is Flip Chip technology where the chip is flipped to lay top down on a ceramic (AlN) substrate as an alternative to the conventional packaging (whether metal or plastic). The ceramic and the GaAs are connected by metal bumps [19,20] which serves as thermal and electrical paths. These bumps are usually Au plated, 15µm to above 30µm height. The lower limit of the bump height is set by mechanical stress due to the existence of thermal expansion mismatch between different materials, the upper limit is set by thermal resistance along with electrical parasitic. This flip chip technology was started by IBM , the C4 process, but solder was used due to its ease of manufaturability (it reflows at lower temperature making it unsuitable to GaAs power amplifier). Sharp is already using flip-chip technology based on Au bump [19].

It is necessary to optimize the layout of the multifinger emitter HBTs and the chip size (~.1-.3mm^2) to lower the thermal resistance and reduce the nonuniformity of current flow in the emitters [20]. The addition of a resistance to the emitter known as ballast restore improves the current distribution but reduces the gain.

Reduction of thermal resistance is a must to avoid thermal runaway and short lifetime. Solutions varies from thinning the III-V substrates to thermal metal shunt with heat spreader and flip-chip (with Plated Au) as new approaches.

7. Examples of current products of HBTs and Future outlook

The cost, low power consumption , the performance along with shorter time-to-market are necessary for HBT products to survive in the semiconductor market and compete against III-V FETs, Si, SiGe, or SOI (Si on Insulator) technology. The high linearity and efficiency of HBTs along with its higher speed and power density make it the best candidate in many 10-100 GHz applications. HBTs are being used in high power microwave amplifier, A/D and D/A converters, multiplexers and demultiplexers, PLLs for communication systems and other high frequency electronic and optoelectronic applications for civil and military purposes [18,21-31]. The mobile communication system (0.9-2 GHz) which represents currently the high volume RF market, uses mainly GaAs MESFETs and Si

devices eventhough HBT has low power consumption [3,4] but its cost is higher.

Si/SiGe HBTs were used in amplifiers at X- and Ku-Band, exhibiting a gain of 4dB at 10 GHZ and 1.4dB at 16.6 GHZ [14], and in active frequency Multipliers at millimeter wave for 55 GHZ with a conversion efficiency better than -12dB [23]. Also, GaAs HBT was used in various Amplifiers up to a 15 GHz bandwidth, in low noise amplifiers (BW of 4.5 GHz), in power amplifier with 1W to 100 W output power [28], in X- and K-Band Mixers and in other up-to-20GHZ ICs [28]. GaAs and InP-based VCO (Voltage Controlled Oscillator) is an active area where a frequency of oscillation of 94.3 GHz with P_{out}=-8dBM were reached [15]. In high speed switching, GaAs can offer higher level of integration then CMOS resulting in a more reliable, cheaper and low power system [30]. HBTs MMICs target is small size chip, low current operation, and low cost. GaAs and InP ICs are needed in satellite communication, automotive radar, PCS system, and single chip radio.

RF system-on-chip solution are heavy-based on Si, it is a hybrid or monolithic integration of Si and other compound semiconductor devices. The rule is to use Si devices if performance requirement is met.

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