Ministry of Higher Education
King Fahd University of Petroleum & Minerals
Electrical Engineering Department

وزارة التعليم العالي
جامعة الملك فهد للبترول و المعادن
قسم الهندسة الكهربائية

EE 203: Electronics I

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Examination: Final Exam

Date : May 19, 2013

Time: 8:00-10:30 AM

Student Name:	
Student Number:	
Section Number:	

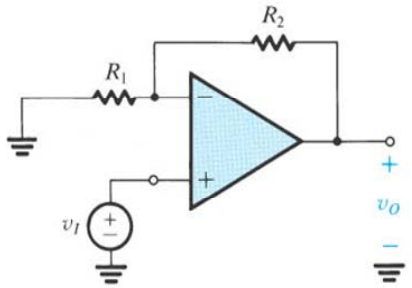
Problem 1	20	
Problem 2	20	
Problem 3	20	
Problem 4	20	
Problem 5	20	
Total	100	

Answer all questions showing all steps. More than one answer for the same problem are given zero mark.

Problem (1) [20 points]

Part 1: Select the correct answer in the following multiple choice questions (MCQs) [1 Mark each].

MCQ 1:
Compared to the inverting op-amp, the main advantage of the non-inverting op-amp shown in the circuit below is:



A. its high output impedance.
B. its high input impedance.
C. its low output impedance.
D. its positive gain.

MCQ 2:
The instrumentation amplifier is a high performance version of:

A. The inverting amplifier.
B. The non-inverting amplifier.
C. The difference amplifier.
D. The weighted summer amplifier.

MCQ 3:
Peak inverse voltage for a diode is

A. Maximum voltage across the diode working in forward direction.
B. Maximum voltage across the diode working in the reverse direction.
C. Minimum voltage across the diode working in the reverse direction.
D. None of the above.

MCQ 4:
The BJT can be used as an amplifier if:

A. The EB junction is reverse biased and CB junction is forward biased.
B. The EB junction is forward biased and CB junction is reverse biased.
C. The EB junction is forward biased and CB junction is forward biased.
D. The EB junction is reverse biased and CB junction is reverse biased.

MCQ 5:
Which of the following amplifier configurations has high input resistance and low output resistance ?

A. Common Emitter amplifier.
B. Common Emitter amplifier with R_s.
C. Common base amplifier.
D. Common collector amplifier.

MCQ 6:
Which of the following relation is correct for BJT in saturation mode?

A. $I_c = \beta I_B$

B. $I_c < \beta I_B$

C. $I_c > \beta I_B$

D. $\beta I_c < I_B$

MCQ 7:

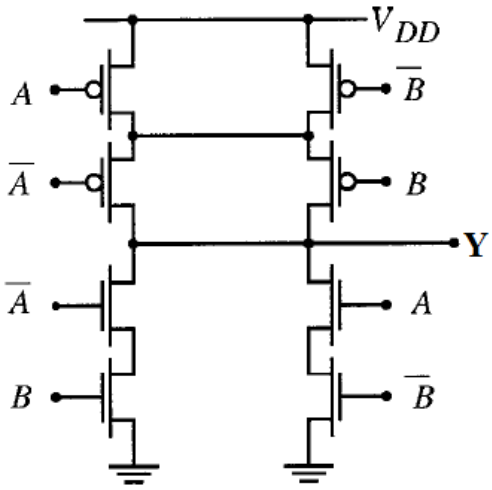
The sizes of PMOS transistors with input A and B in terms of the size of PMOS transistor of the basic inverter **p** are:

A. M_A=1**p**, M_B=1**p**

B. M_A=1**p**, M_B=2**p**

C. M_A=2**p**, M_B=1**p**

D. M_A=2**p**, M_B=2**p**



MCQ 8:
When the MOSFET operates in triode region it has a resistance r_{DS} which is:

A. Proportional to (W/L).

B. Proportional to $1/(W/L)$.

C. Proportional to $(W/L)^2$.

D. Proportional to $1/(W/L)^2$.

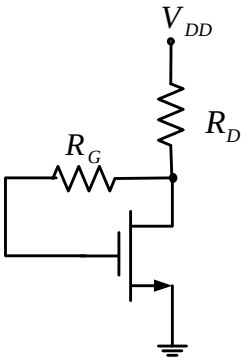
MCQ 9:
Biasing the MOSFET as shown in the figure will place the transistor in:

A. In the border between saturation (pinch-off) and triode regions.

B. In the saturation (pinch-off) region when R_D is greater than R_G.

C. In the saturation (pinch-off) region when V_{DD} is greater than V_t.

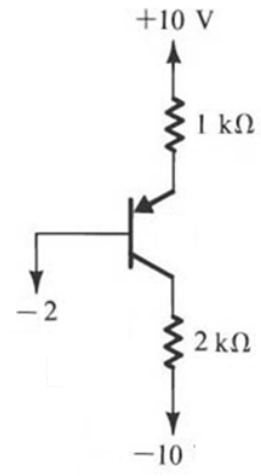
D. In the saturation (pinch-off) region when R_D is less than R_G.



Part 2: Fill in the blank (FIB) with correct values:

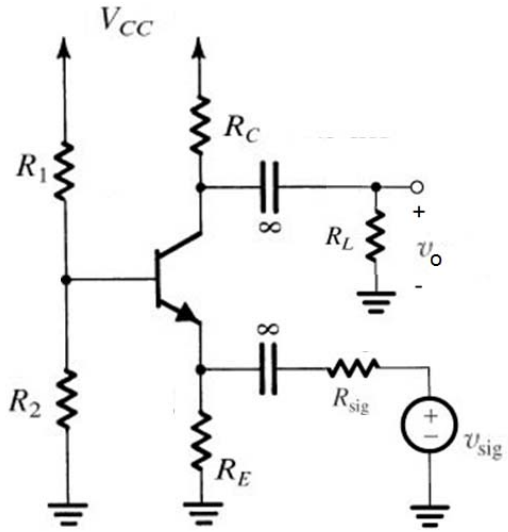
FIB 1 [4 Marks]:

The transistor in the circuit below has β=100, V_{EB} (on) = 0.7V and $V_{ES\ (sat)}$ = 0.2V. Given that the transistor is working in saturation, then the collector voltage V_C = …….



FIB 2 [4 Marks]:

The input resistance of the amplifier is given by R_{in}=……..



FIB 3 [3 Marks]:
The VTC of an inverter is shown below, determine corresponding

V_{OH} =……V

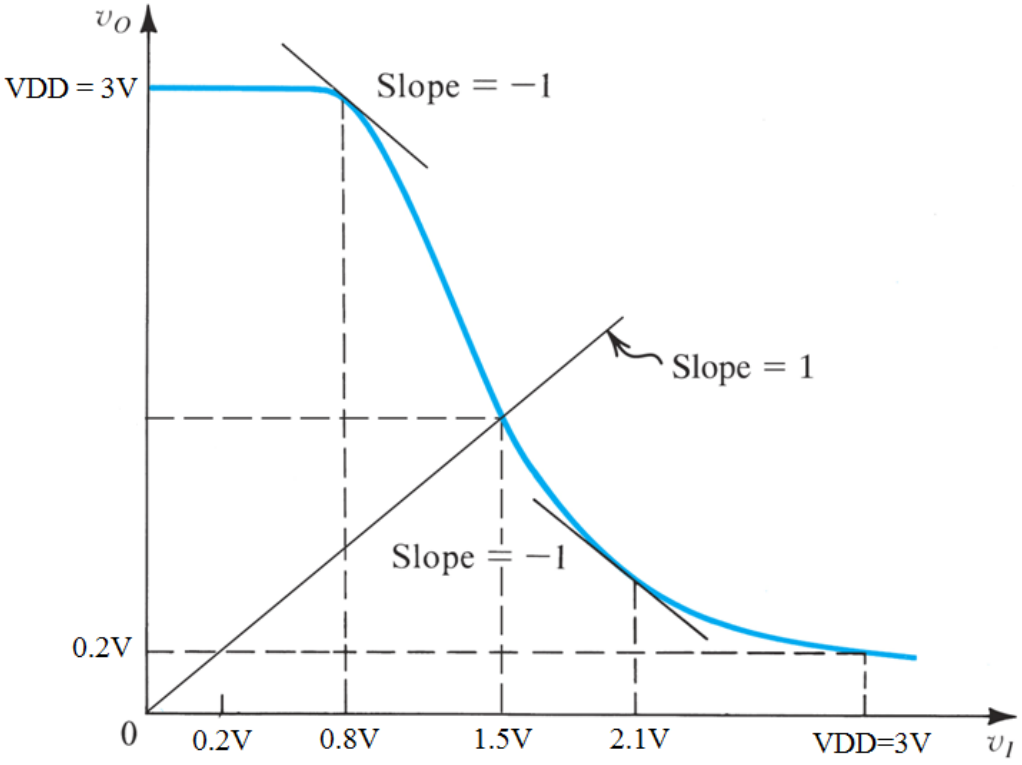
V_{OL} = ……V

V_{IL} =……V

V_{IH} = ……V

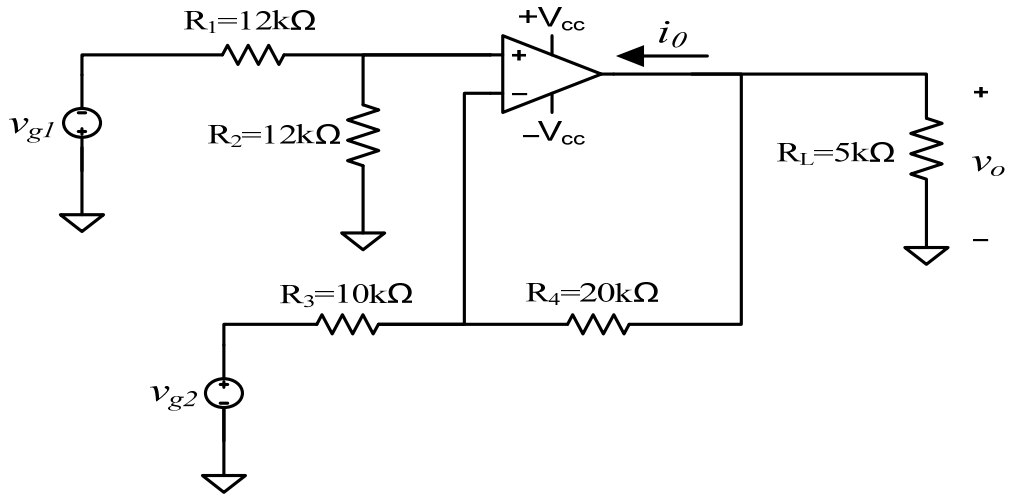
V_{NMH} = ……V

V_{NML} = ……V

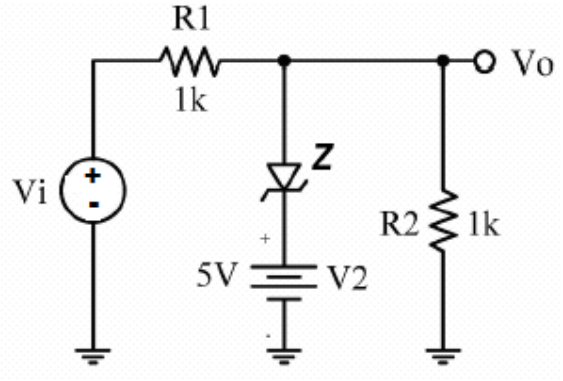


Problem (2) [20 points]

A. For the ideal op-amp circuit show in the figure,
Find the expression of the output voltage v_o as a function of the input voltages v_{g1} and v_{g2}.



B. For the circuit shown below, assume that the zener diode has **Vz=3.3V** and **rz=0Ω** when reverse biased, and has a 0.7V drop when forward biased. Fill the following table for values of Vo for different values of input voltage Vi.

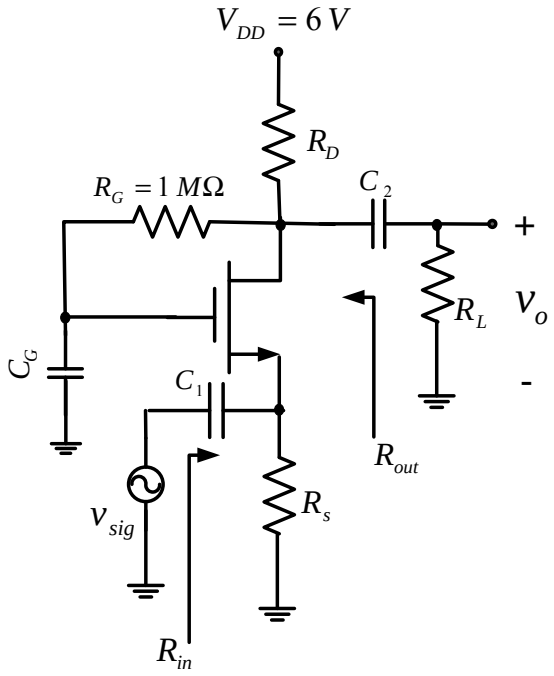


Vi	Vo
-8V	
0V	
8V	

Problem (3) [20 points]

The CMOS in the amplifier circuit shown below has $V_t = 1.5\ volt$, $k_n' \frac{W}{L} = 2\ mA/V^2$. The current $I_D = 0.81\ mA$ and $R_D = R_L = R_s = 2\ k\Omega$. Neglecting the output resistance r_o of the transistor, determine:

(a) DC biasing voltages (V_{GS} , V_{DS}).
(b) Draw the small signal equivalent circuit.
(c) The input resistance R_{in} .
(d) The voltage gain v_o / v_{sig} .
(e) The output resistance R_o .

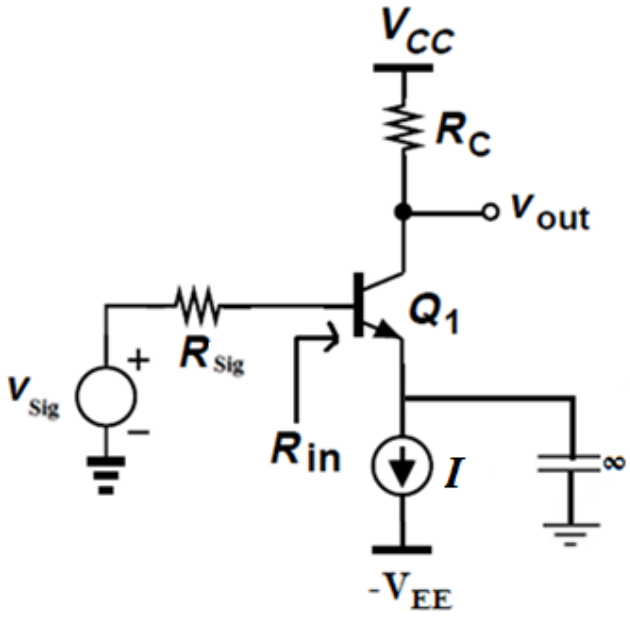


Problem (4) [20 points]

Consider the circuit shown below, with the BJT transistor operating in active region. Select the value of the DC current '**I**' and the value of the resistor '$\mathbf{R_C}$' such that:

R_{in} = 5kΩ, $\frac{v_{out}}{v_{sig}} = -75 \frac{V}{V}$,

Neglect r_o and assume β=100, R_{sig} =1kΩ and $V_{CC} = V_{EE}$ = 5V.

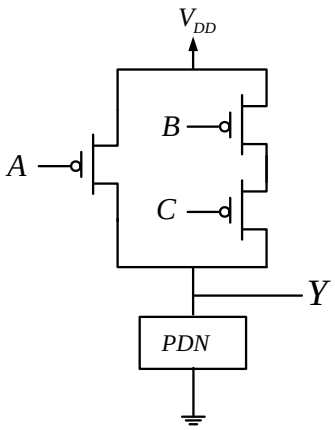


Problem (5) [20 points]

1. In addition to Fan-In and Fan-Out, list another four of the main design parameters of logic gates.

   (i)
   (ii)
   (iii)
   (iv)

2. Determine the logic function Y realized by the given logic gate.



3. Design a CMOS logic gate with minimum number of transistors to implement the function X. Then expand the design to implement the logic function Y with minimum number of transistors as well.

$$X = \overline{(A + B).C}$$

$$Y = \overline{\left((A + B).C.D\right) + E}$$

4. Design a 2 by 1 multiplexer using pass transistor logic (Transmission gates) that selects one of four inputs from A and B depending on the selection bit S1.
Draw the complete circuits shown all transistors including the inverter.