King Fahd University of Petroleum & Minerals
Electrical Engineering Department
Fall 2011 (111)

EE 203 – Final Exam
Monday, January 16, 2011
7:00-10:00 PM

Name	
ID	

	Dr. W. Mesbah	Dr. O. Hammi
Section	1 and 2	3 and 4

Problem	**1** **(out of 10)**	**2** **(out of 10)**	**3** **(out of 10)**	**4** **(out of 10)**	**5** **(out of 10)**	**6** **(out of 10)**	**Total** **(out of 60)**
Grade							

Important:

- **Final answers must be written in the specified boxes. The steps should be included.**

Problem 1 – Part A

For the circuit shown in Figure 1-A, the voltage drop across each conducting diode is 0.7V.

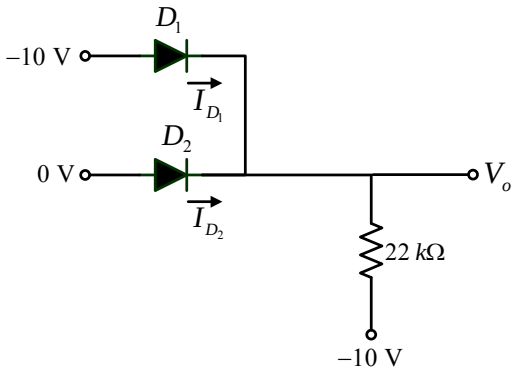


Figure 1-A

a) Find the output voltage V_o .**[2 points]**

V_o=

---

b) Find the current I_{D1} .**[1 point]**

I_{D1}=

---

c) Find the current I_{D2} .**[1 point]**

I_{D2}=

Problem 1 – Part B

For the circuit shown in Figure 1-B, the Zener diode has a voltage drop of 9.1V at 9mA, r_z=30Ω, and I_{zk}=0.3mA.

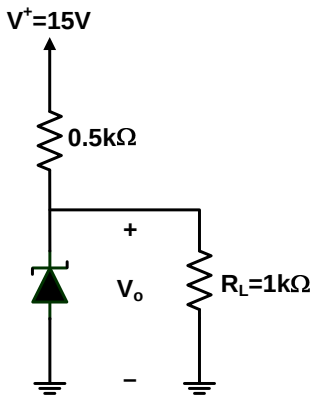


Figure 1-B

a) Find the output voltage V_o with no load connected.
[2 points]

V_o=

---

b) Find the output line regulation with no load connected.**[2 points]**

---

c) For what range of values of R_L , the diode still operates in the breakdown region. (For this part, assume r_z=0Ω).**[2 points]**

Problem 2

For the amplifier shown in Figure 2, assume that the NMOS has V_t=1V, $\mu_n C_{ox} W/L$=1mA/V^2, and λ=0.01V^{-1}.

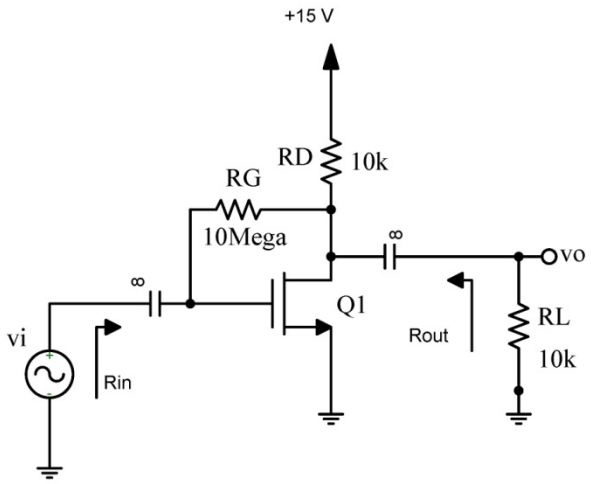


Figure 2

Sketch the DC circuit here

a) Sketch the DC circuit in the designated box. **[1 point]**

b) Neglecting the effect of λ (**only in this part**), calculate the DC values I_{DS} and V_{DS}. **[2 points]**

I_{DS}=

V_{DS}=

---

c) Calculate the small-signal parameters g_m and r_0. **[2 points]**

g_m=

r_0=

d) Draw the small-signal AC circuit using the **π model** of the transistor. **[2 points]**

e) Use the small-signal ac circuit to write the expressions of R_{out} , R_{in} , and the gain v_o/v_i (for the gain calculation **ONLY**, assume $R_G=\infty$). **[3 points]**

$R_{out}=$

$R_{in}=$

$v_o/v_i=$

Problem 3:

Consider the circuit shown in Figure 3. The BJT transistor has β=100. Neglect the Early effect.

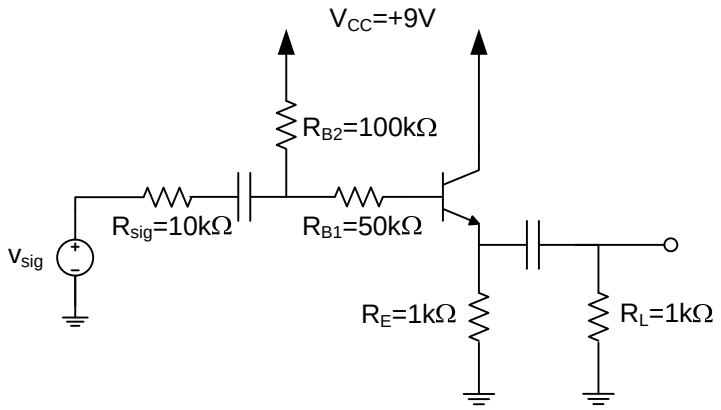


Figure 3

a) Draw the small signal equivalent circuit using the transistor's **T model**. **[2 points]**

b) Find the expressions of the input resistance R_{in} and the output resistance R_{out} of the amplifier.**[2 points]**

R_{in}=

R_{out}=

---

c) Calculate the values of the input resistance R_{in} and the output resistance R_{out} of the amplifier.**[2 points]**

R_{in}=

R_{out}=

---

d) Find the expression of the voltage gain v_{out}/v_{sig} in terms of R_{in} and/or R_{out}.(Do not replace R_{in} and/or R_{out} by the expression found in question b)) **[2 points]**

$v_{out}/v_{sig} =$

---

e) If the voltage v_{be} should not exceed 5mV. What is the maximum input voltage v_{sig_max}. **[2 points]**

$v_{in\_max} =$

Problem 4:

Consider the circuit of Figure 4. The transistors Q_1 and Q_2 have $k'_nW/L = 2.5$ mA/V^2 , $V_t = 1$ V, and $\lambda = 0$. The DC current through R_{ss} is1 mA.

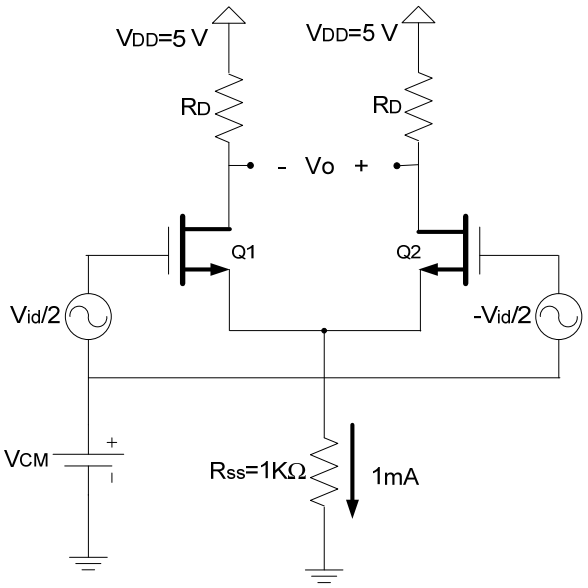


Figure 4

Sketch the DC circuit here

a) Sketch the DC circuit in the designated box. **[2 points]**

b) Find the required value of the DC voltage V_{CM} .**[2 points]**

V_{CM}=

c) Find the value of R_D that results in a differential gain A_d of -8 V/V. **[2 points]**

R_D=

---

d) Determine the DC voltage at the drain of Q_1. **[2 points]**

V_D=

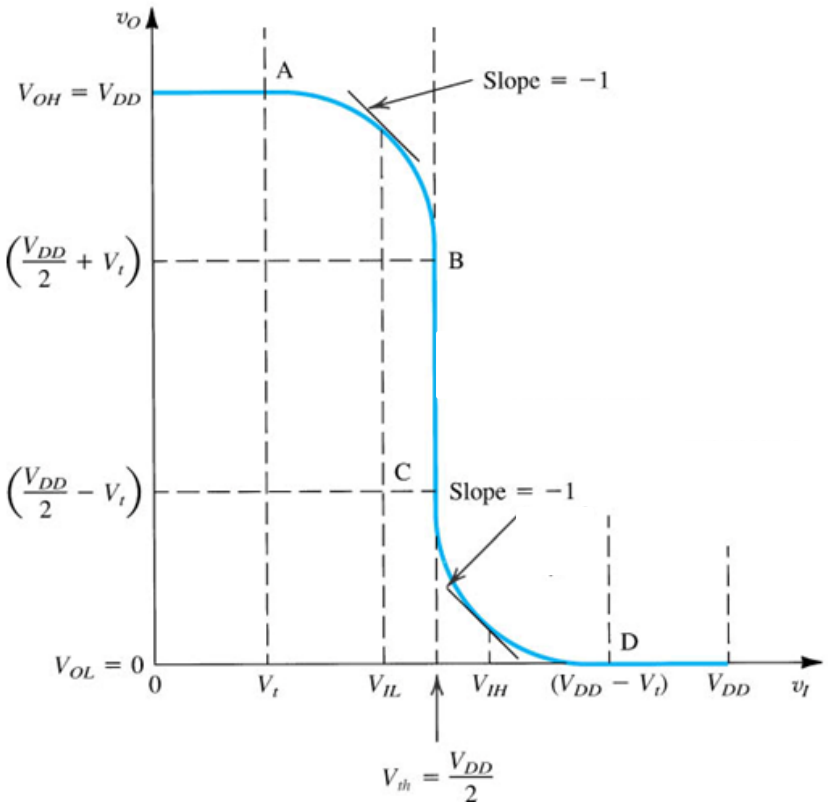
---

e) Calculate the single-ended common mode gain (for an ac input signal). **[2 points]**

A_{CM}=

Problem 5 – Part A:

Consider the voltage transfer function of the CMOS shown in Figure 5-A. Indicate, **on the same figure**, the mode of operation of the NMOS and PMOS transistors in each region of the voltage transfer characteristic. Clearly show the limits of each region. **[5 points]**



Problem 5 – Part B:

a) What is the minimum number of transistors required to implement the following logic function using CMOS gates. **[2 points]**

$Y = A\overline{B}C + ABC + AB\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C$

Minimum number =

---

b) If "**p**" represent W/L of the PMOS of the basic inverter, design the PUN and the sizing of each transistor (show the sizes on the PUN circuit) for the function: $Y = \overline{B}C + B\left(A + \overline{A}\overline{C}\right)$. **(Do not simplify or change the equation. You do not have to plot the inverters). [3 points]**

Problem 6:

Consider the ECL circuit shown in Figure 6. The transistors used have V_{BE}=0.7V at I_E=1mA. The current I_{tot}=4mA all the time. Neglect the base currents when collector currents are present. Assume that $\beta_{Q2}=\beta_{Q3}=100$. Consider only the **OR** output at the emitter of Q_2.

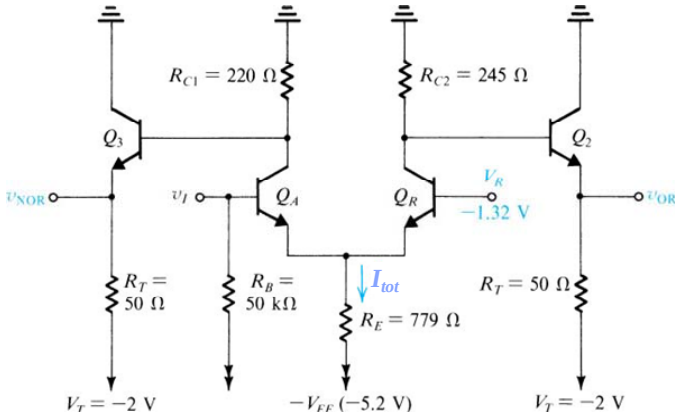


Figure 6

a) If we define the voltages V_{IL} and V_{IH} when the current in one branch is **95%** of I_{tot}. Calculate the voltages V_{IL} and V_{IH} for the OR output. **[4 points]**

V_{IL}=
V_{IH}=

b) Calculate the voltages V_{OL} and V_{OH} for the OR output. **[4 points]**

V_{OL}=

V_{OH}=

---

c) Calculate the noise margins N_{ML} and N_{MH} for the OR output. **[2 points]**

N_{ML}=

N_{MH}=