King Fahd University of Petroleum & Minerals

Electrical Engineering Department

EE 203 (102) – Final Exam

Tuesday, Jun 14, 2011

7:00-9:30 PM

Name	
ID	

	Dr. Oualid	Dr. Al-Gahtani	Dr. Al-Zaher	Dr. Wessam
Section	1 , 2	3, 6	4 , 5	7 , 8

Question	**Grade**
1 [25 Marks]	
2 [10 Marks]	
3 [15 Marks]	
4 [15 Marks]	
5 [20 Marks]	
6 [15 Marks]	
Total [100 Marks]	

Question: 1

A. [15 Marks]

For the circuit shown in Fig. 1, the transistors parameters are: $V_{TN} = 1V$, $\mu_n C_{ox} = 44.4\mu A/V^2$, $\lambda = 0$, and $L = 1\mu m$.

Assume Q1, Q2 and Q3 are identical.

i) Determine the value of V1**.**

ii) Design the transistors sizes (find W3) such that V2= 3V.

iii) Determine the mode of operation of each transistor.

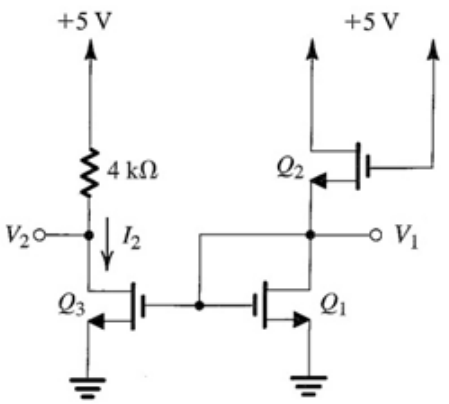


Fig 1

B. [10 Marks]

For the circuit shown in Fig 2,

- For the BJT assume $V_{BE}=0.7V$ and neglect the base current (Large β)
- The NMOS transistor has $V_t=1V$, **$\lambda = 0$** and $\mu C_{ox} W/L = 2mA/V^2$.
- Assume Q1 is in saturation (pinch off) and Q2 is in active.

i) Find the DC currents I1 and I2 .

ii) Verify the assumption made for the mode of operations.

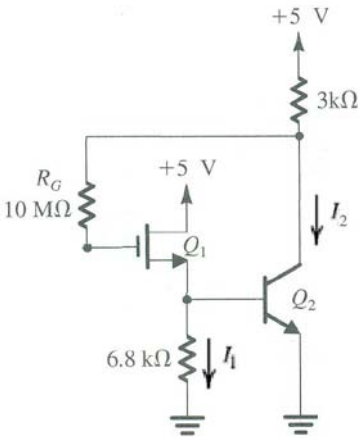


Fig 2

Question: 2

A. [5 Marks]

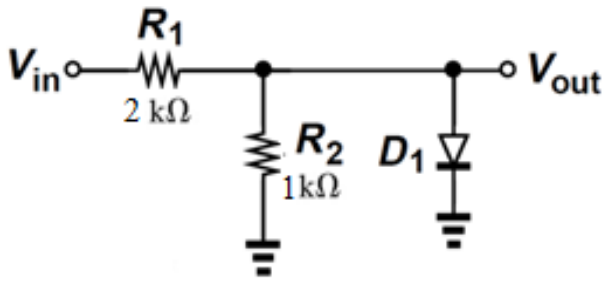
Draw a circuit that can convert 110V AC voltage to DC voltage of 10V.

(The values of the circuit components are not required)

B. [5 Marks]

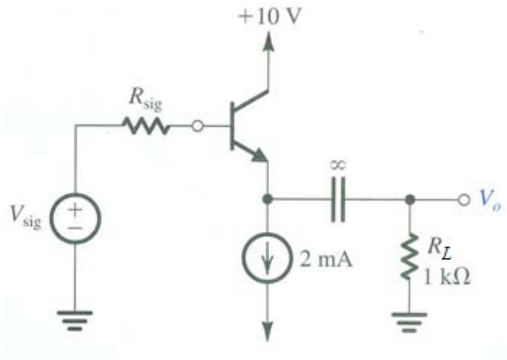
Using the constant-voltage model with $V_D = 0.7V$ plot the Input/output characteristics of the circuit shown below.

(Label all the critical voltage levels)



Question: 3 [15 Marks]

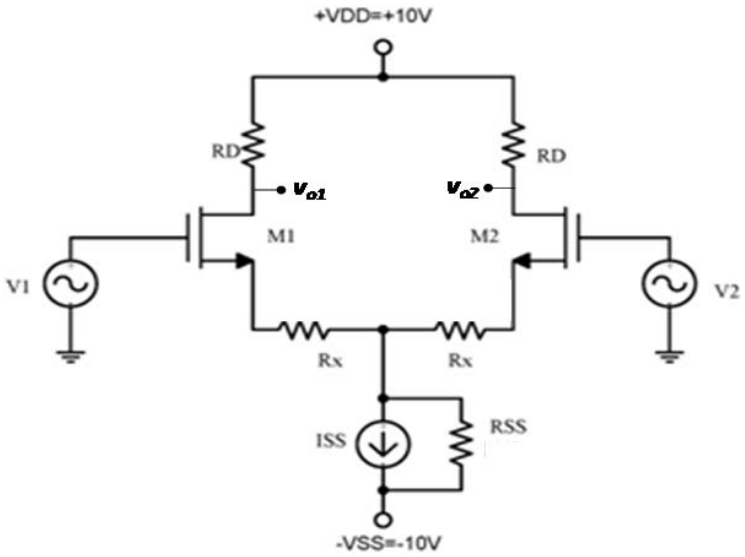
For the emitter follower shown, let $\beta=100$ and $R_{sig}=10k\Omega$.



- **A.** Calculate the collector current I_C.
- **B.** Draw its small signal equivalent circuit.
- **C.** Calculate the model parameters.
- **D.** Find the voltage gain v_o/v_{sig}.
- **E.** Find the input resistance.
- **F.** Find the output resistance

Question 4: [15 Marks]

For the shown differential amplifier assume identical transistors with $V_1=v_{cm}+ v_{id}/2$ **&** $V_2=v_{cm}- v_{id}/2$. Assume $\lambda = 0$.



A. Draw the small signal equivalent half-circuit for **the differential mode**

B. Draw the small signal equivalent half-circuit for **the common mode.**

C. If the output is taken single-ended (v_{o2} from M_2 drain), find the expressions of **A_d, A_{cm} and CMRR.**

D. If the output is taken differentially ($v_{o2} - v_{o1}$), find the expressions of **A_d, and A_{cm}.**

Question: 5

A. [15 Marks]

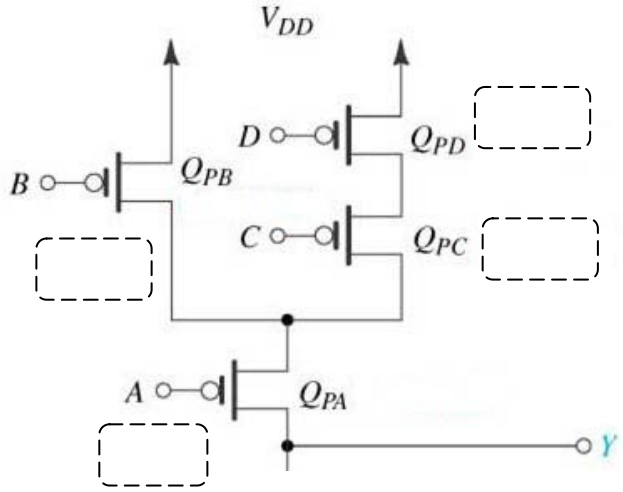
For the shown pull-up network:

i) Draw the corresponding pull-down network.

ii) Write an expression for output Y in terms of the inputs A, B, C and D

Y=

iii) On each transistor, show the correct sizing $\frac{W}{L}$ of the pull-up network in terms of $p = \frac{W}{L}$ of the basic inverter



B. [5 Marks]

Design a pass-transistor logic (transmission gate) circuit to realize the following function:

The output Y equals to the input A if the input C is high and the output Y equals the input B if the input C is low.

[Draw the complete transistor level circuit]

Question: 6 [15 Marks]

For the shown ECL gate, assume all transistors are in active and neglect the base currents. If V_R= -1.85V, I=1mA, R=2.3kΩ and the all the transistors have V_{BE}=0.7V for a 1mA emitter current.

(a) What is the logic function performed at V_{o1}?

(b) If V_B is sufficiently negative to turn Q_B off and V_A is connected to V_i, calculate

i. VIL, and VIH?

VIL=

VIH=

ii. VOL, and VOH?

VOL=

VOH=

iii. NMH, and NML?

NMH =

NML =