EE200 DIGITAL LOGIC CIRCUIT DESIGN

Class Notes
CLASS 15-1

The material covered in this lecture will be as follows:

⇒Synchronous counters.

- Binary counter.
- Up-down counter.
- BCD counter.

After finishing this lecture, you should be able to:

⇒ Understand the principles used in the design of synchronous binary counters.

⇒ Change up counters to down counters.

⇒ Use the design procedure of synchronous sequential circuits to design BCD counter and other modulus-N counters.

Synchronous Counters

Synchronous counters can be designed using the design procedure of the clocked sequential circuits. The count pulses are applied to the clock inputs of all flip-flops of the counter. Therefore the changes in the outputs occur at the same time. Several typical synchronous counters are presented in this section and their operation explained.

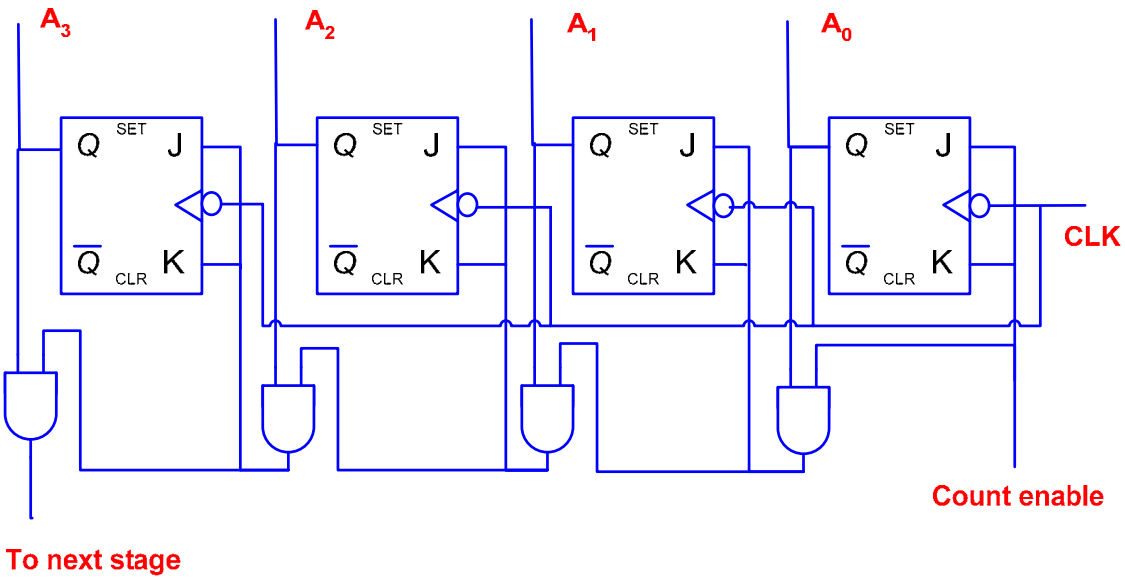
Synchronous binary counter

The operation of the synchronous binary counter is so simple and follows an easy complementing pattern that a simple design procedure can be followed. There is no need to follow the general procedure for the design of synchronous sequential circuits. If we inspect the count cycle or the timing diagram of the binary counter we find the following:

1. A_0 complements every time the count pulses go from 1 to 0.
2. A_1 complements only when A0 is 1 and goes to 0.
3. A_2 complements only when A1 and A0 are 1 and going to 0.
4. A_3 complements only when A_2, A_1 and A_0 are all 1 and going to 0.

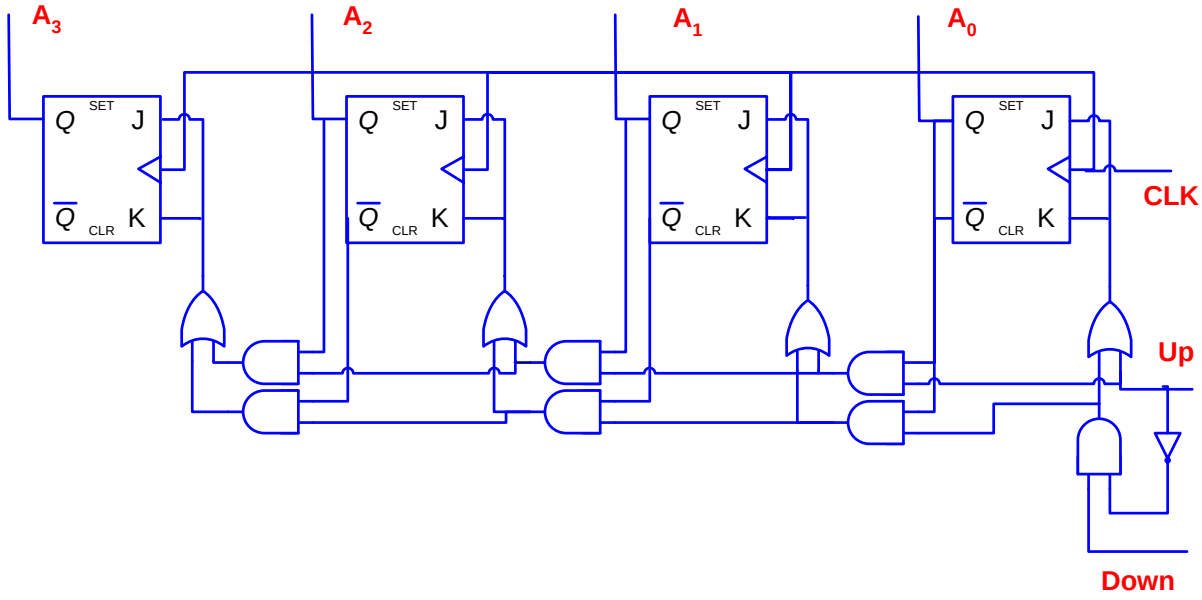
From this pattern it becomes clear that the J and K inputs of flip-flop A0 should be kept at 1 (the count enable can be used in stead of 1). The count enable is Anded with A0 and applied to the J and k inputs of A1. This pattern is repeated by Anding the J and K input of each flip-flop with the flip-flop output and applied to the J and K inputs of the next flip-flop.

The logic circuit of a modulus-16 synchronous binary counter using JK flip-flops is given next.



Up-Down Counter

The down counter counts in reverse from 1111 to 0000 and then goes to 1111. If we inspect the count cycle, we find that each flip-flop will complement when the previous flip-flops are all 0 (this is the opposite of the up counter). The down counter can be implemented similar to the up counter, except that the AND gate input is taken from Q' instead of Q. This is shown in the following Figure of a 4-bit up-down counter using T flip-flops.



BCD Synchronous Counter

The BCD counter does not have a regular pattern. Therefore we have to follow the design procedure of synchronous sequential circuits. Using T flip-flops, the state table of the counter will be given as follows:

P.S.				N.S.					Flip-flop inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	T_8	T_4	T_2	T_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

The flip-flop input equations can be simplified by means of Karnaugh maps:

$$T_1 = 1$$

$$T_2 = Q_8' Q_1$$

$$T_4 = Q_2 Q_1$$

$$T_8 = Q_8 Q_1 + Q_4 Q_2 Q_1$$

And $y = Q_8 Q_1$