The material covered in this lecture will be as follows:

⇒Ripple counters.

- Binary ripple counter.
- BCD (Decimal) ripple counter.

After finishing this lecture, you should be able to:

⇒ Describe the operation of binary ripple counters.

⇒ Recognize the count cycle and timing diagram of counters.

⇒ Understand the modifications required for the input functions to transform the 4-bit binary ripple counter to BCD ripple counter.

Ripple Counters

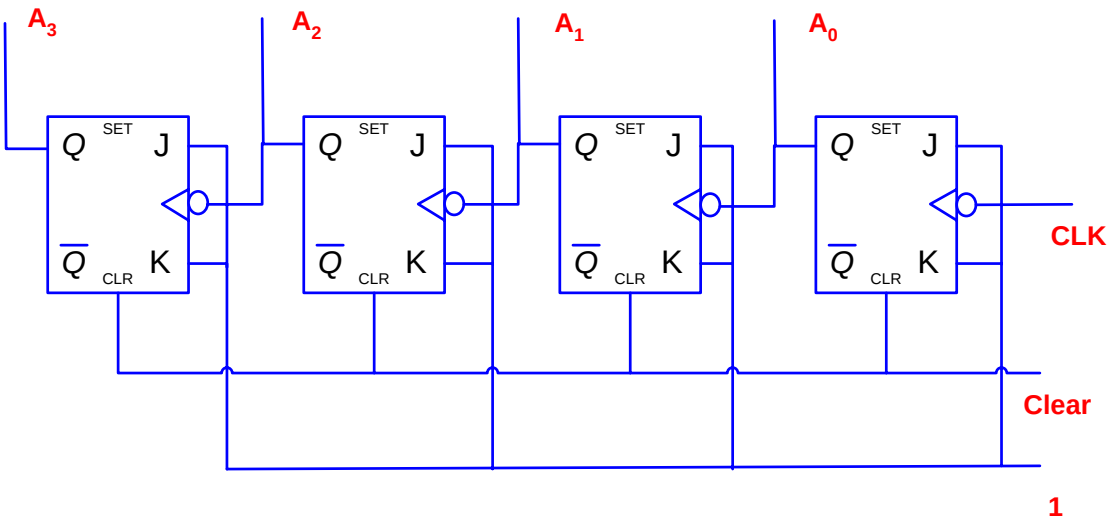
There are two categories of counters:

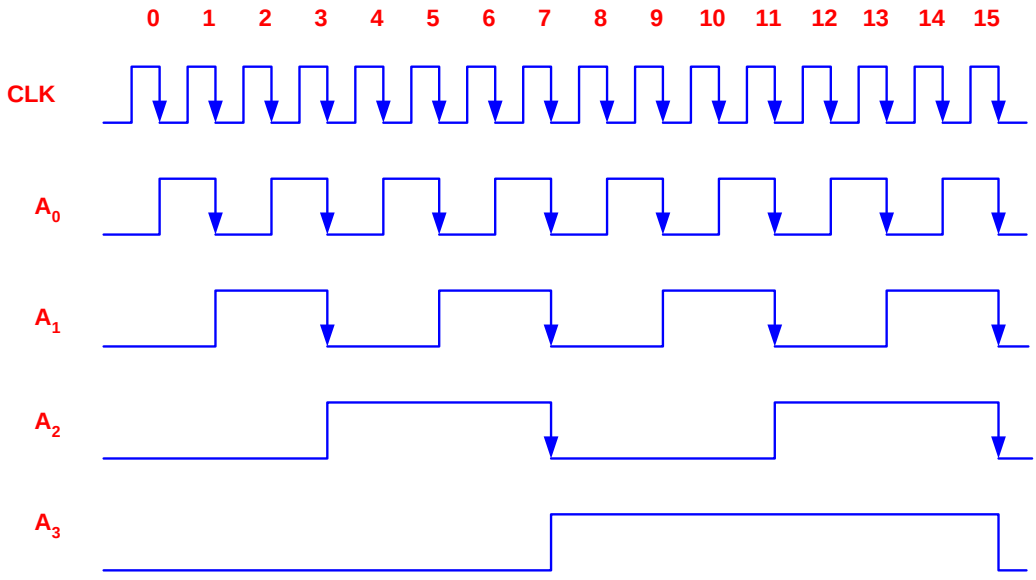
- Ripple counters,
- Synchronous counters.

Ripple counters are counters where each flip flop is triggered by the transition of other flip-flops. In synchronous counters all flip-flops are triggered by the same clock pulses.

Binary Ripple Counter

Binary ripple counter consists of a series of complementing flip-flops. A binary counter consisting of n flip-flops has a count cycle of 2^n and counts from 0 to 2^n-1. A 4-bit binary ripple counter using T flip-flops is shown.

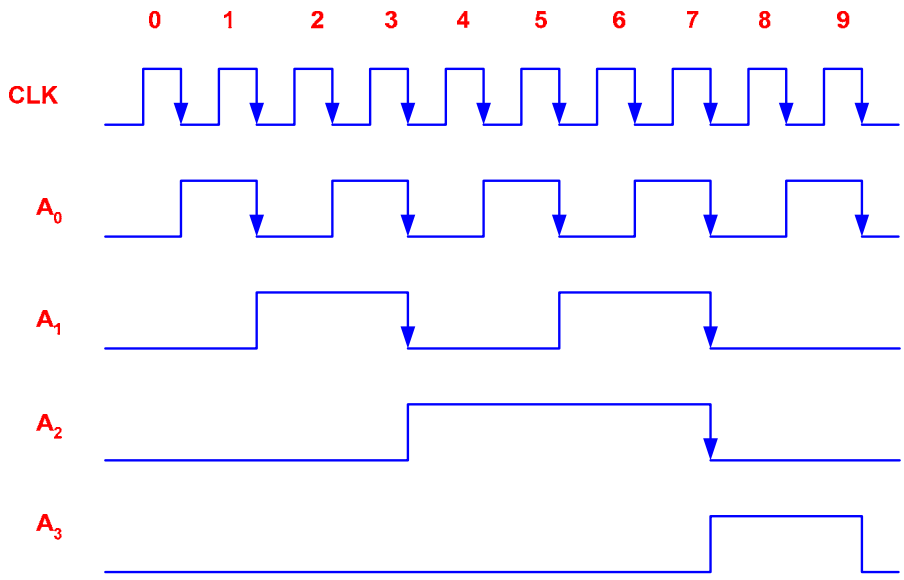




Timing Diagram of the 4-bit ripple counter

BCD Ripple Counter

The BCD ripple counter has a modulus of 10. It counts from 0 to 9 and then resets to 0. The timing diagram of this counter is shown. The main difference between this timing diagram and that of the binary counter is that A1 and A3 reset after the 10th pulse.



Timing Diagram of the BCD ripple counter

In order to arrive at the design of the BCD ripple counter, we must answer two questions concerning each flip-flop:

1. Which source should trigger the flip-flop?
2. What values should we make the J and K inputs of the flip-flop?

Using the timing diagram, it is clear that A_0 is to be triggered by the input clock pulses and the J and K inputs should be made 1 and 1. A_1 should be triggered by A_0. In order to prevent it from

setting on the negative edge of pulse 9, we should make the J and K inputs equal to A_3' and 1. A_2 is triggered by A_1 and the J and K inputs are 1 and 1. Finally, A_3 should be triggered by A_0. TO

prevent A_3 from setting until we reach pulse 7, then we should make the J and K inputs equal to A_2A_1 and 1. The logic circuit of the BCD ripple counter is shown next.