

EE200 DIGITAL LOGIC CIRCUIT DESIGN

The material covered in this **lecture** will be as follows:

- ⇒ Serial addition.
- ⇒ Universal shift register.

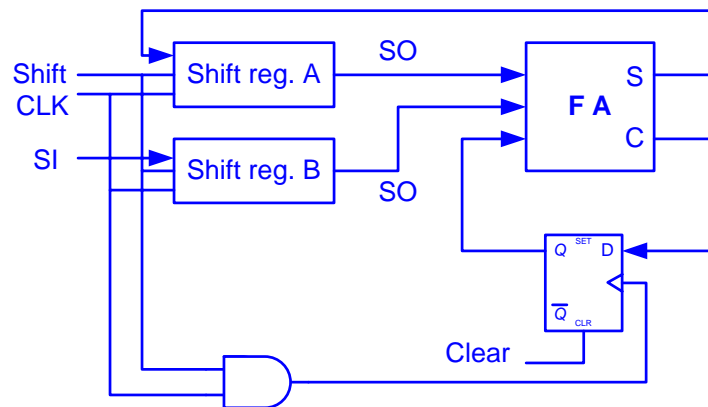
After finishing this lecture, you should be able to:

- ⇒ Describe the main functions of registers and counters.
- ⇒ Differentiate between shift registers and registers with parallel load.
- ⇒ Understand the serial transfer operation in registers.
- ⇒ Understand the operation of the universal shift register.

Serial Addition

We are going to investigate the operation of a serial adder in comparison to the parallel adder.

The two binary numbers to be added serially are stored in shift registers A and B. The carry of the full adder is stored in a D flip-flop and used as the carry-in with the next pair of bits to be added. The sum bit is shifted in shift register A to replace the first number. At the end of the number of clock pulses used to add the two numbers, the sum will be available in register A. Register B can be made to contain a third number to be added to the sum. This process can be repeated any number of times to add more than two numbers. The serial adder is shown in the following Figure.



Design of the Serial Adder

The serial adder can be designed using the design procedure of the clocked sequential circuits.

We wish to design a sequential circuit that can add two bits x and y provided by two shift registers together with a carry bit that can be obtained from the output Q of a storage element (flip-flop), and produces the sum bit that can be stored in a shift register and the carry bit that can be added to the next pair of bits.

The number of inputs is $n=2 \rightarrow x$ and y

The number of outputs is $m=1 \rightarrow S$

One flip-flop is needed to provide the carry-in for the addition. Let us choose a JK flip-flop. This description of the problem can be translated directly into a state table as follows:

P.S.	Inputs		N.S.	Output	Flip-Flop inputs	
Q	x	y	Q	S	J	K
0	0	0	0	0	0	X
0	0	1	0	1	0	X

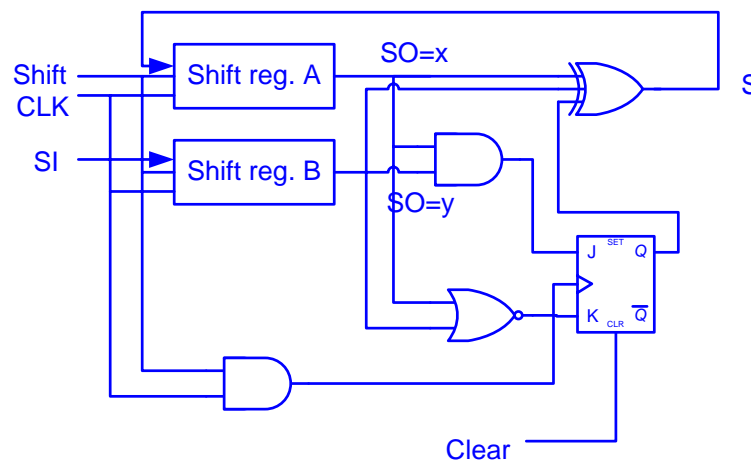
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

The output and flip-flop input functions are then given by:

$$S = x \oplus y \oplus Q$$

$$J = xy \quad \text{and} \quad K = x'y' = (x + y)'$$

The circuit diagram consists of three gates and one flip-flop as shown in the following diagram.



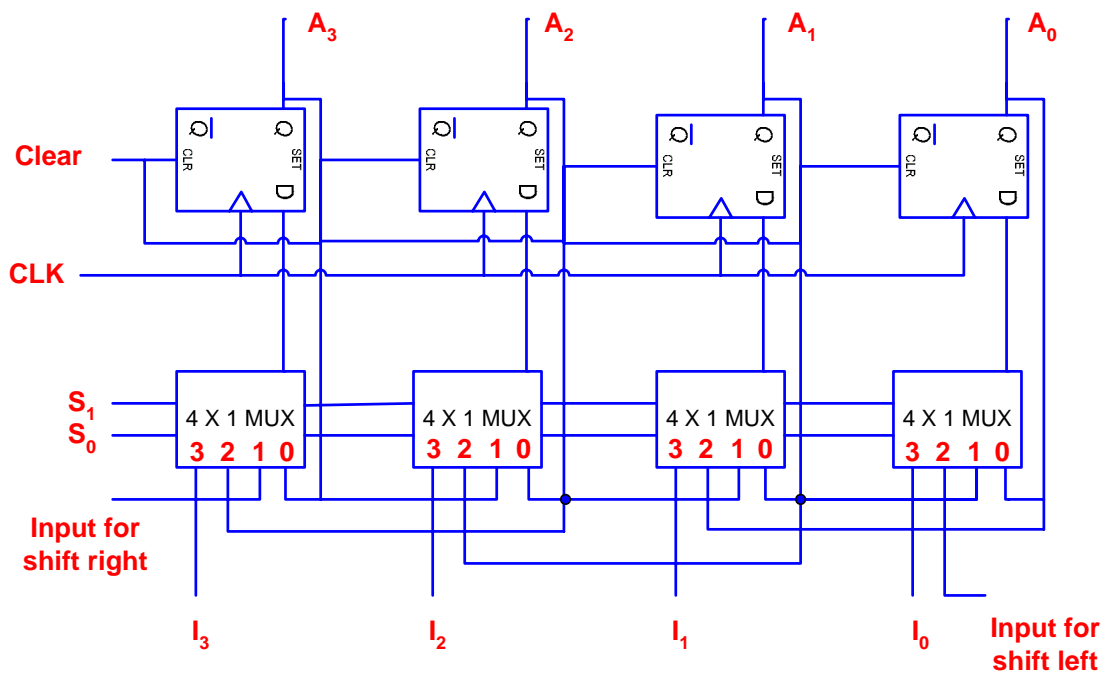
Universal Shift Register

Registers are available in integrated circuit form that can function as shift register in either direction (right or left), register with parallel load. Data can also be kept in the register while the clock pulses are applied. This universal register has the following capabilities:

1. A clear (reset) input.

2. A clock input.
3. A shift right control.
4. A shift left control.
5. A parallel load control.
6. A control input to keep the contents of the register unchanged while clock pulses are applied.

A universal shift register that has the previous capabilities is constructed using D flip flops and multiplexers. The construction of a 4-bit register is shown in the following diagram.



The function table for this register is given below.

Mode Control		Operation
S ₁	S ₀	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load