The material covered in this lecture will be as follows:

⇒ Design of clocked sequential circuits using D flip-flops.

⇒ Design of clocked sequential circuits using JK flip-flops.

⇒ Design of a binary counter using T flip-flop.

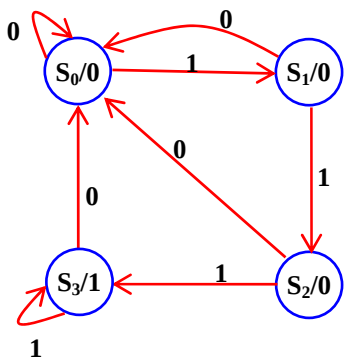
After finishing this lecture, you should be able to:

⇒ Design a clocked sequential circuit using any type of flip-flops.

⇒ Design clocked synchronous counters using any type of flip-flops.

Design of a Sequence Detector using D Flip-Flops

The state diagram and the state table of the sequence detector are given below



P.S.		Input	N.S.		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

We use two D flip-flops with the four states 00, 01, 10, and 11. The next state is equal to the flip-flop input. The state table may be considered as a truth table for the combinational circuit part.

The required functions are D_A, D_B, and the output y.

$$D_A(A,B,x) = \sum(3,5,7)$$

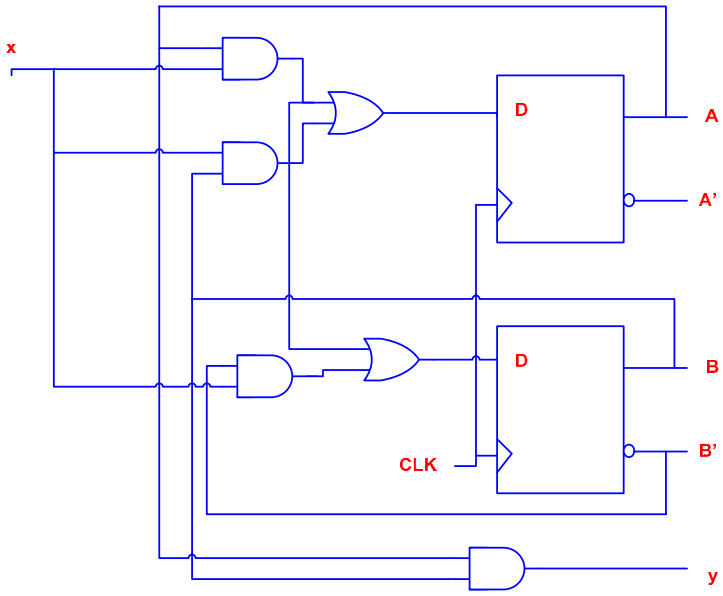
$$D_B(A,B,x) = \sum(1,5,7)$$

and $y(A,B,x) = \sum(6,7)$

These functions can be simplified and the logic circuit drawn.

$$D_A = Ax + Bx$$
$$D_B = Ax + B'x$$
$$y = AB$$

And the logic circuit is shown next.



Design of Clocked Sequential Circuits Using JK Flip-Flops

When selecting the JK flip-flop in the design of clocked sequential circuits, we must use the excitation table of the flip-flop in order to obtain the flip-flop input functions. The following example illustrates the procedure:

Example of The Design Using JK Flip-Flops

Design the clocked sequential circuit that has the following state table using JK flip-flops.

P.S.		Input	N.S.	
A	B	x	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

We use the excitation table of the JK flip-flop in order to obtain the input functions of the flip-flops. The state table becomes the excitation table of the sequential circuit.

P.S.		Input	N.S.		Flip-Flop Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

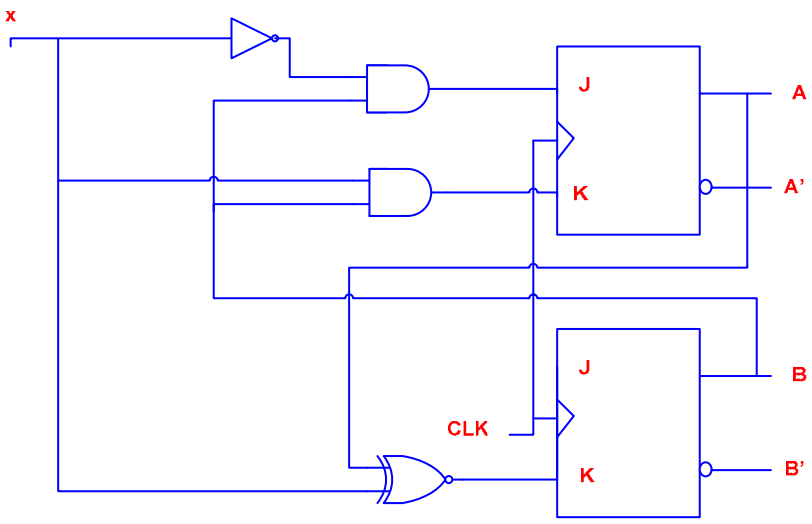
The excitation table can now be treated as a truth table for the combinational circuit part. We can obtain the Boolean expressions of the required functions and simplify them using Karnaugh maps.

$$J_A = Bx' \qquad K_A = Bx$$

and

$$J_B = x \qquad K_B = A'x' + Ax = (A \oplus x)'$$

The logic circuit can then be drawn.

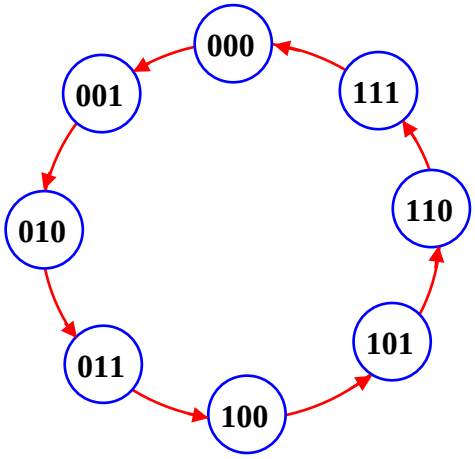


Design of a Binary Counter Using T Flip-Flops

We are going to design a binary counter as an example for the synthesis procedure using T flip-flops.

A binary counter of n flip-flops will be able to count from 0 to a maximum count of 2^n-1. As an example a binary counter comprising three flip-flops will count from 000 to 111 and then resets to 000. We wish to design such counter using T flip-flops.

The state diagram of such counter is shown.



The excitation table of the circuit, which is shown next, consists of the state table together with the flip-flop input functions which can be completed with the aid of the T flip-flop excitation table.

P.S.			N.S.			Flip-Flop Inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

From the table, and using Karnaugh maps for simplifications, we get:

$T_{A2} = A_1 A_0$ $T_{A1} = A_0$ and $T_{A0} = 1$

The logic diagram is shown.