The material covered in this lecture will be as follows:

⇒Design procedure.

⇒Flip-flop excitation tables.

⇒Design of a sequence detector.

After finishing this lecture, you should be able to:

⇒ Design a clocked sequential circuit from a verbal description of its function.

⇒ Use the excitation table of a given flip flop in the design of the sequential circuit.

Design Procedure

1. Derive a state diagram from the verbal description.
2. Reduce the number of states, if necessary.
3. Assign binary values to the states.
4. Obtain the state table.
5. Choose the type of flip-flops.
6. Derive the simplified flip-flop input equations and output equations.
7. Draw the logic diagram.

Flip-Flop Excitation Tables

In the design of clocked sequential circuits, we know the present state and next state of the flip-flops. We need to find the flip-flop input functions and the output functions in order to design the combinational circuit part of the circuit. These functions can be easily obtained using the flip flop excitation table. These tables

give us the required inputs that will achieve a given transition from Q_t to Q_{t+1}.
The excitation table of the three types of flip-flops are:

D Flip-Flop Excitation Table

Q_t	Q_{t+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

JK Flip-Flop Excitation Table

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T Flip-Flop Excitation Table

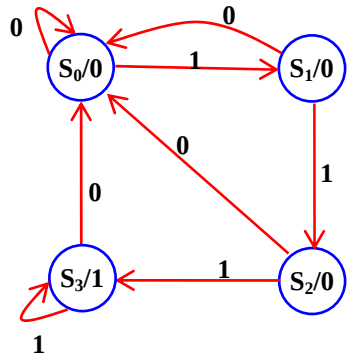
Q_t	Q_{t+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Design of a Sequence Detector

We wish to design a circuit that detects three or more consecutive 1's in a string of bits coming through an input line. We start in the

initial state S_0. If the input is 0 then the circuit stays in S_0. the first input 1 will take the circuit to the next state S_1. Any input 0 will take the circuit back to state S_0. Only three consecutive 1's will take the circuit through the states S_0, S_1, S_2, and S_3. Any further 1's will leave the circuit in state S_3.

The state diagram is shown below



Synthesis using D flip-flops

The state diagram is used to prepare the state table which is shown below.

P.S.		Input	N.S.		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1