The material covered in this lecture will be as follows:

⇒State reduction.

⇒State assignment.

After finishing this lecture, you should be able to:

⇒ Recognize when state reduction is needed.

⇒ Understand why state reduction is performed.

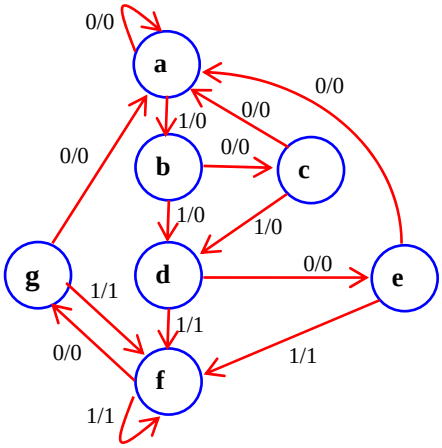
⇒ Perform state reduction on state tables.

⇒ Perform state assignment.

State reduction

In the design of sequential circuits, we need to reduce the number of flip flops and the number of logic gates used in the combinational circuit part. Reduction of the number of flip-flops may result from the reduction of the number of states in the circuit. This is possible if we are interested in the input output relationship of the circuit and not in the outputs of the flip-flops.

The state reduction procedure will be illustrated with an example. Consider the given state diagram



Suppose that the input sequence to the circuit is 01010110100 starting from the initial state a. Then the output and next state will be as follows:

State	a	a	b	c	d	e	f	f	g	f	g	a
Input	0	1	0	1	0	1	1	0	1	0	0	
Output	0	0	0	0	0	1	1	0	1	0	0	

The pattern is as shown here: → P.S. Input Output → N.S.

The state table can be arranged as follows:

P.S.	N.S.		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

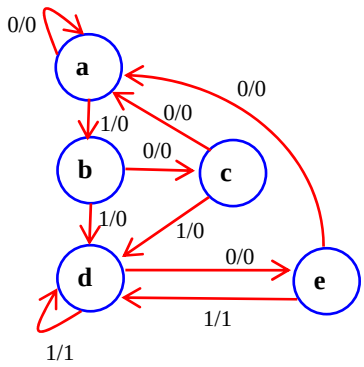
States g and e are identical then we can cancel state g and substitute e for g in the table. This will reduce the states from 7 to 6. Next, we find that states d and f are identical. Then we cancel f and replace it in the table with d. No further reduction is possible.

The number of states has been reduced from 7 to 5. No reduction in the number of flip-flops is possible, because we need 3 flip-flops for 5 states, which is he same number of flip-flops for 7 states.

The reduced state table will be as follows:

P.S.	N.S.		Output	
	x = 0	x = 1	x = 0	x = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

And the reduced state diagram will be as follows:



The input sequence will result in the same output sequence using the reduced state table or diagram as shown in the following table.

State	a	a	b	c	d	e	d	d	e	d	e	a
Input	0	1	0	1	0	1	1	0	1	0	0	
Output	0	0	0	0	0	1	1	0	1	0	0	

The reduction of the number of states could lead to reduction of the number of flip-flops or it might not lead to it. WSe started in the previous example with seven states, which need 3 flip-flops in the design of the circuit. We managed to reduce the number of states to five. The number of flip-flops needed is still 3.

State assignment

We need to assign coded binary values to the different states in the state table. In the previous example, we have 5 states and three flip-flops. We must choose five combinations out of the total of 8 possible combinations. 3 combinations will not be used and can be considered don't care conditions. Examples of state assignments are given in the following table.

State	Assign.1	Assign. 2	Assign.3
a	000	000	011
b	001	001	100
c	010	011	101
d	011	010	110
e	100	110	111