EE200 DIGITAL LOGIC CIRCUIT DESIGN

Class Notes
CLASS 11-3

The material covered in this lecture will be as follows:

⇒Positive edge triggered D flip-flop.

⇒Characteristic tables.

⇒JK and T flip-flops.

⇒Direct inputs.

After finishing this lecture, you should be able to:

⇒ Understand the operation of the positive edge triggered D flip flop.

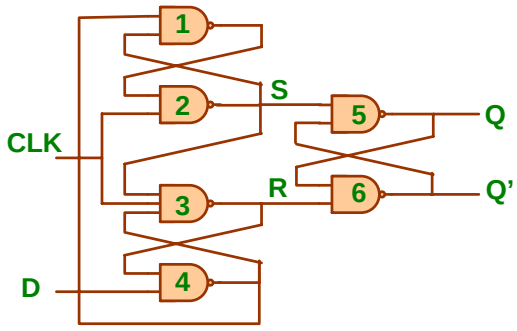
⇒ Understand the operation of the JK and T flip flops.

⇒ Appreciate the importance of the characteristic tables of flip flops and how they are different from the truth tables of combinational circuits.

⇒ Recognize the need of direct inputs for flip flops and understand how they are implemented.

Positive Edge triggered D Flip-Flop

The positive edge triggered D flip-flop consists of three basic SR latches. This arrangement is shown in the logic diagram.

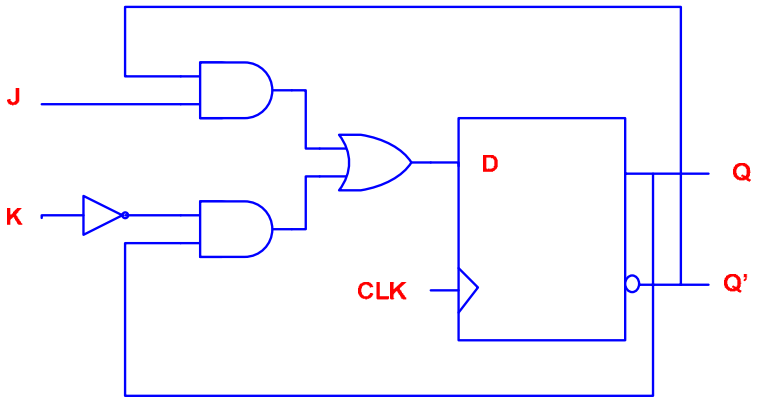


When CLK=0 and D=0, then the outputs of gates 1, 2, 3, and 4 are going to be 0111. If D=1 while CLK=0, then the outputs of these gates are going to be 1110 instead. In both cases, S=R=1, which make Q and Q' are 01 or 10. i.e. one of the two stable states.

Suppose that CLK becomes 1 while D=0. The output of gate 3 (which is R) becomes 0. this will reset the output flip-flop. Once R is 0, then D can change to 1 and R remains 0. This means that Q remains 0 while CLK is 1. No change will occur to Q until the clock returns to 0 and then goes to 1 on the next clock pulse. This scenario shows that the flip-flop is a positive edge triggered.

Similar procedure occurs if D=1 while the clock goes from 0 to 1. In this case, S=0 and Q=1.

JK Flip-Flop



The D input is given by: $D = JQ' + K'Q$

The characteristic equation of the JK flip-flop is:

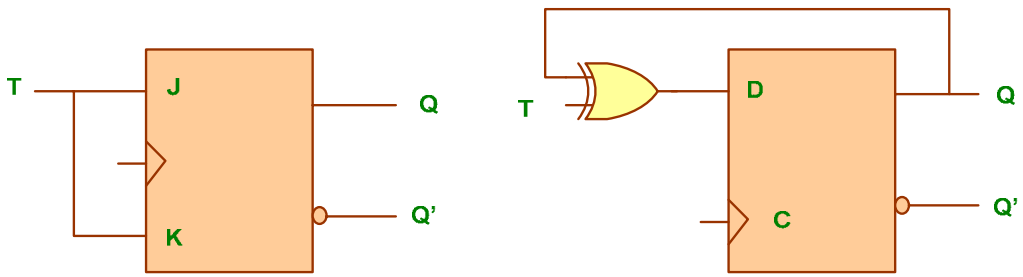
$$Q_{t+1} = JQ' + K'Q$$

The characteristic table of the JK flip-flop is given below.

J	K	Q_{t+1}	
0	0	Qt	No change
0	1	0	Reset
1	0	1	Set
1	1	Q_t'	Complement

T Flip-Flop

A T flip-flop is obtained from the JK flip-flop by connecting J and K together to form a single input T. The T flip-flop is a toggling (complementing) one if T is kept at 1. It can also be obtained from a D flip-flop and an exclusive-OR gate as shown in the Figure.

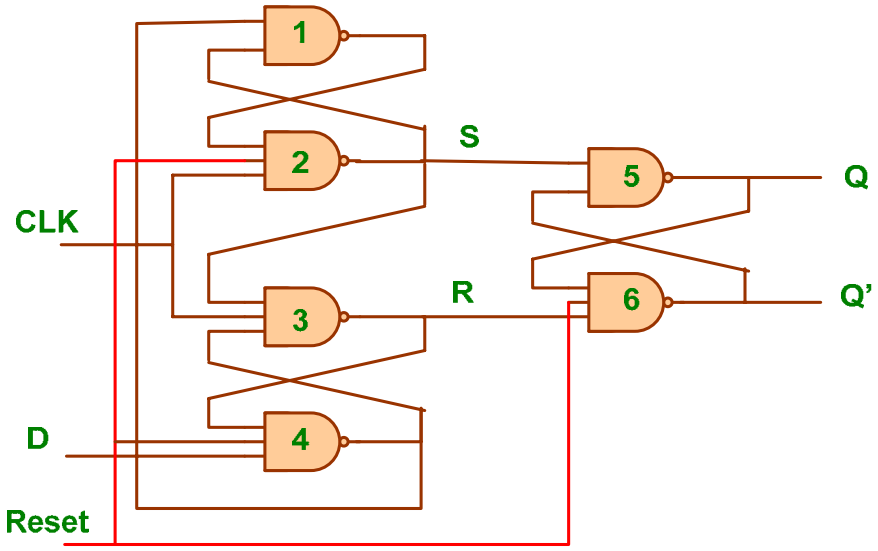


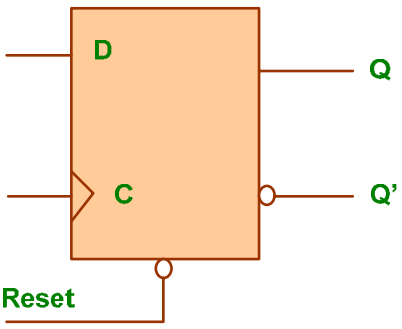
The characteristic equation of the T flip-flop is given by:

$$Q_{t+1} = T \oplus Q = TQ' + T'Q$$

Direct Inputs

These are asynchronous inputs that can reset or set the flip-flops at any time without the application of clock pulses.





Reset	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0