EE200 DIGITAL LOGIC CIRCUIT DESIGN

Class Notes
CLASS 11-1

The material covered in this lecture will be as follows:

⇒Triggering of flip-flops.

⇒Edge triggered flip-flops.

⇒Master-slave D flip-flop.

⇒Positive edge triggered flip-flop.

⇒Characteristic tables.

After finishing this lecture, you should be able to:

⇒ Understand the main types of triggering of flip flops.

⇒ Realize the importance of edge triggering.

⇒ Understand the concept of master/slave connection and how it results in negative edge triggering.

Triggering Of Flip-Flops

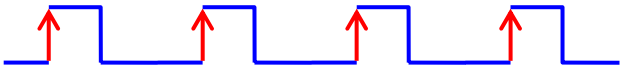
The D latch is triggered with clock pulses when the clock goes from o to 1. The outputs can change as long as the clock is at level 1. This type of triggering is called “Level triggering”. The problem with level triggering is that the outputs of the latches change all the time while the trigger is 1. It becomes difficult to predict the final outputs of the latches in the sequential circuit and consequently, common clock source cannot be applied to all the latches in the circuit at the same time.

This problem can be solved by using edge triggering instead of level triggering. There are two type of edge triggering:

1. Positive edge triggering.
2. Negative edge triggering.

These are shown in the following Figure.

Level Triggering



Positive Edge Triggering

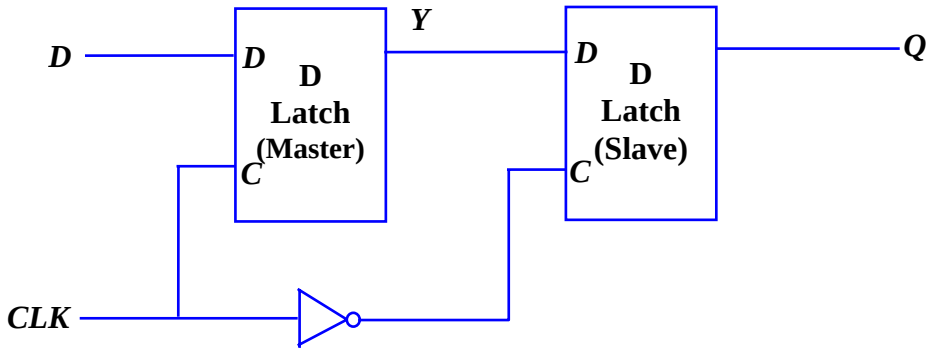
Negative Edge Triggering

Edge Triggered D Flip-Flops

There are two types of edge triggered flip-flops:

1. Master-slave flip-flop.
2. Positive edge triggered D flip-flop.

The Master-Slave D Flip-Flop



The following timing diagram shows how the output Q of the master-slave D flip-flop changes on he negative edge of the clock pulse.