

EE200 DIGITAL LOGIC CIRCUIT DESIGN

The material covered in this class will be as follows:

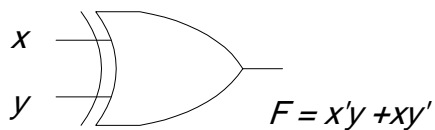
⇒ Exclusive-OR function.

⇒ Parity Generation and Checking.

EXCLUSIVE-OR FUNCTION

The exclusive-OR (XOR), denoted by the symbol \oplus , is a logical operation that performs the following Boolean operation:

$$x \oplus y = xy' + x'y$$

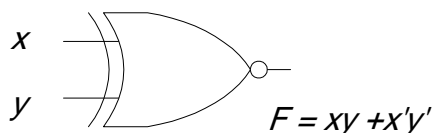


x	y	$x \oplus y$
0	0	0
0	1	1
1	0	1
1	1	0

XOR Truth Table

The exclusive-NOR, also known as equivalence function, performs the following Boolean operation:

$$x \ominus y = xy + x'y'$$



x	y	$x \ominus y$
0	0	1
0	1	0
1	0	0
1	1	1

XNOR Truth Table

The following identities apply to the XOR operation:

$$x \oplus 0 = x$$

$$x \oplus 1 = x'$$

$$x \oplus x = 0$$

$$x \oplus x' = 1$$

$$x \oplus y' = x' \oplus y = (x \oplus y)'$$

$$x \oplus y = y \oplus x$$

$$(x \oplus y) \oplus z = x \oplus (y \oplus z)$$

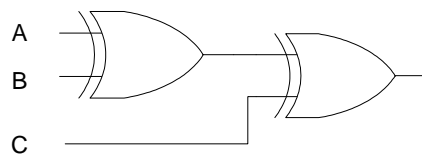
The exclusive-OR operation with three and four variables can be expressed as

$$A \oplus B \oplus C = \Sigma(1,2,4,7)$$

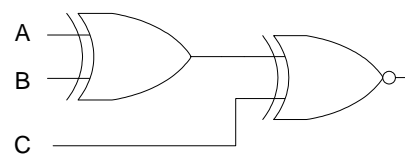
$$A \oplus B \oplus C \oplus D = \Sigma(1,2,4,7,8,11,13,14)$$

We can see from the above expressions that the XOR function is 1 only when an odd number of variables are equal to 1. Hence, in general, the multi-variable XOR operation is defined as the odd function.

The 3-input odd function is implemented by means of 2-input XOR gates as shown below. The complement of an odd function is obtained by replacing the output gate with an XNOR gate.



3-input Odd function



3-input even function

Parity Generation and Checking

Exclusive-OR gates are useful for generating and checking a parity bit that is used for detecting/correcting errors during transmission of binary data over communication channels.

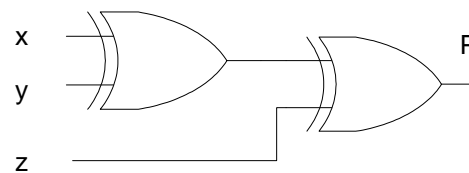
Example

Transmitting a 3-bit message with even parity bit. The three bits – x , y , and z constitute the message and are the inputs to the circuit. The parity bit P is the output, which is an odd function and can be expressed as:

$$P = x \oplus y \oplus z$$

The truth table and the logic diagram for the parity generator is shown below.

Message			Parity
x	y	z	
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

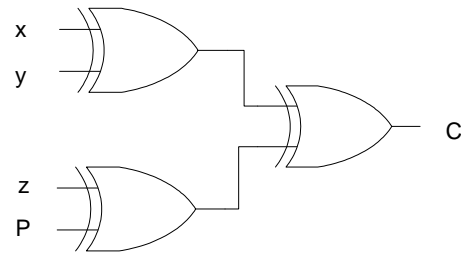


3-bit even parity generator

The three bits in the message together with the even parity bit P are transmitted. The receiver at the destination checks for even number of 1's in the 4-bit message and generates an error C equal to 1 if the number of 1's in the message is odd. Here, again, we can use the odd function property of the XOR gate that produces

an output of 1 if odd number of inputs is equal to 1. The truth table and the logic diagram for the parity checker is shown below.

4-bit Received Message				Error
x	y	z	P	C
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



4-bit even parity checker