EE200 DIGITAL LOGIC CIRCUIT DESIGN

The material covered in this lecture will be as follows:

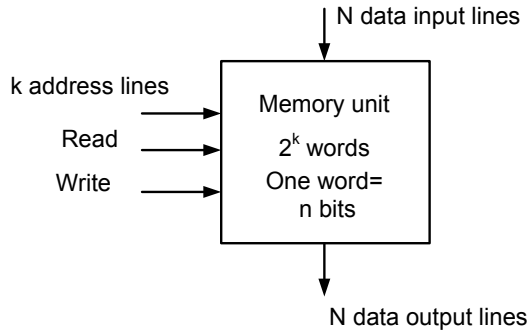
- ⇒Memory and RAM (Random Access Memory)
- ⇒Programmable logic devices.
- ⇒Read Only Memory (ROM).
- ⇒Introduction to Programmable Logic Array (PLA).

After finishing this lecture, you should be able to:

- ⇒ Differentiate between RAM and ROM
- ⇒ Identify programmable logic devices and understand their usage.
- ⇒ Understand the structure and size of the ROM.
- ⇒ Implement Boolean functions using ROM's
- ⇒ Recognize the array logic graphic symbol and appreciate its usage in large programmable logic devices.

Random-Access Memory

RAM is a memory unit which is a collection of storage cells, together with the associated circuits needed to transfer information into and out of the device (WRITE and READ operations respectively).



$1k = 2^{10} = 1024,$
$1M = 2^{20} = 1048576$
$1\ G = 2^{30} = 1.0737x10^{+009}$

Thus, $64k = 2^{16}$,
$2M = 2^{21}$,
and $4G = 2^{32}$

Consider a memory unit of 1 k words of 16 bits each. The arrangement of the memory will be as follows:

Memory address	Memory content
0	10110111 01101101
1	01100101 11100110
3	11101000 10010101
-	-----
-	-----
-	-----
1021	11001011 11000100
1022	10100010 01001010
1023	00010011 10010111

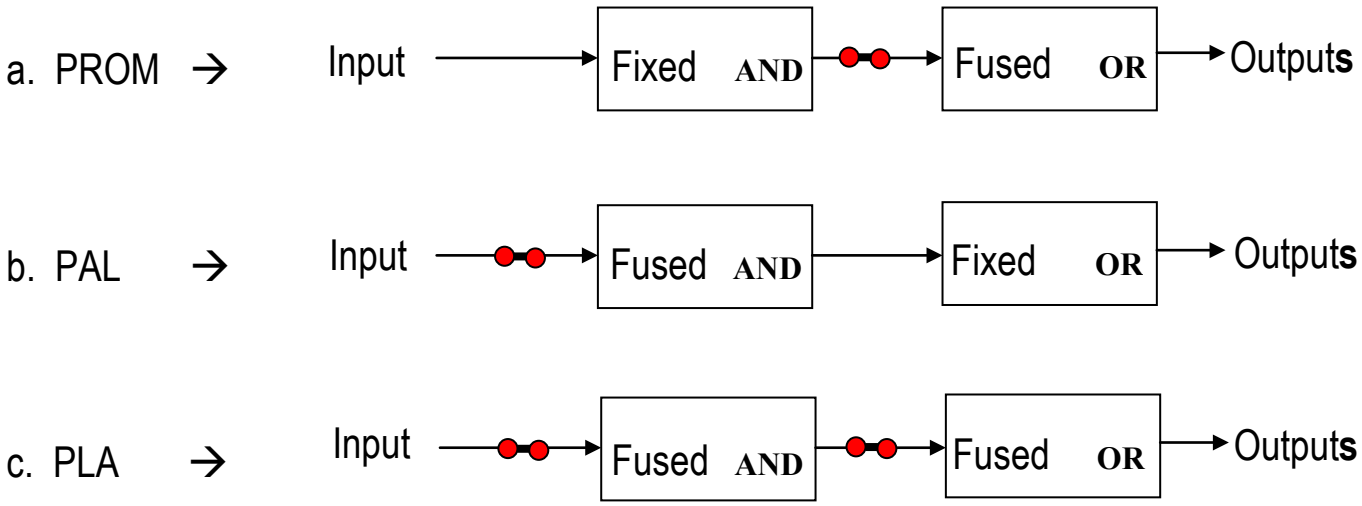
Programmable Logic Devices (PLD's)

Introduction:

Integrated circuits; MSI and PLD packages.

1. As studied before, Integrated circuit categories are: SSI, MSI, LSI, and VLSI. MSI devices have a complexity of approximately 10 to 1000 gates in a single package.
2. Several combinational circuits are available in MSI form, e.g. adders, subtractors, comparators, decoders, encoders, multiplexers,… etc.
3. Programmable Logic Devices are IC's with internal logic gates (arrays of AND gates and OR agates) connected through fuses to establish a pattern of connections.
4. Three types of PLD's are studied here:

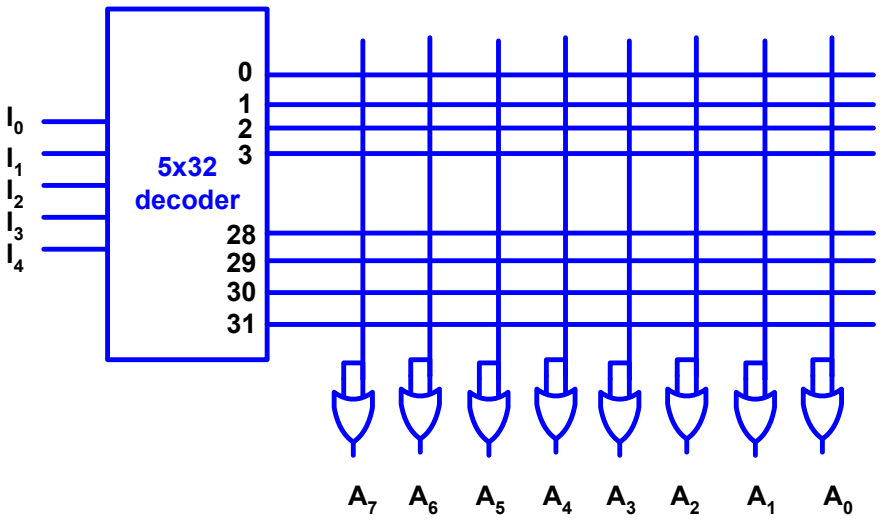
    a. Programmable Read Only Memeory (PROM)
    b. Programmable Logic Array (PLA)
    c. Programmable Array Logic



Read Only Memory (ROM)

A ROM is considered a programmable device where binary information can be stored and kept even when power supply is switched off.

A ROM consists of a decoder and array of fused (programmed) OR gates. This is shown in the following Figure.

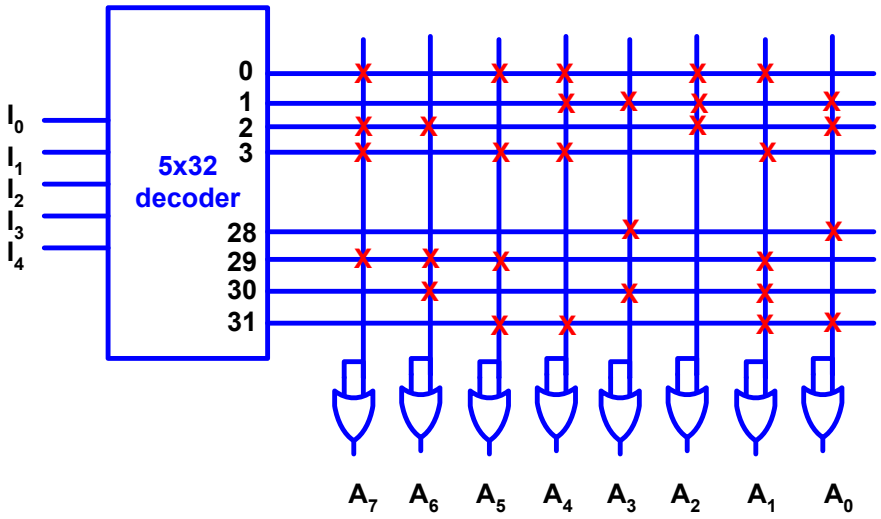


Internal logic of a 32 X 8 ROM

The ROM truth table shows the pattern of the fuses as programmed inside the ROM. The following truth table is an example for the 32 X 8 ROM.

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
…					…							
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

A cross indicates a connection (1), and no cross indicates (0) as shown in the following diagram.



Example

Design a combinational circuit using ROM that accepts a three bit number and generates an output equal to the square of the input number.

All what we do is generate a truth table for the required circuit. Most times this is all what is needed. On some occasions, we may be able to reduce the number of outputs required from the ROM.

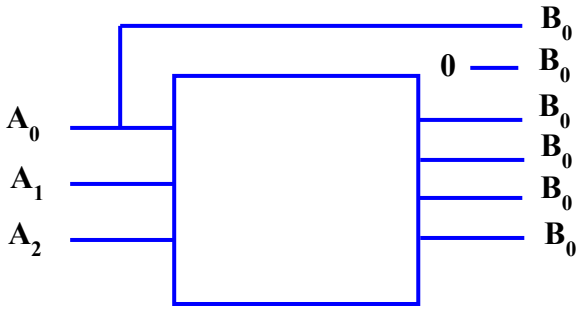
For this circuit we require six outputs, because the largest output is the binary equivalent of $7^2 = 49 \rightarrow 110001_2$.

The truth table

Inputs			Outputs						
A2	A1	A0	B5	B4	B3	B2	B1	B0	Dec.
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

We can find from the table that $B_0 = A_0$, and $B_1 = 0$

The size of the required ROM is 8 X 4.

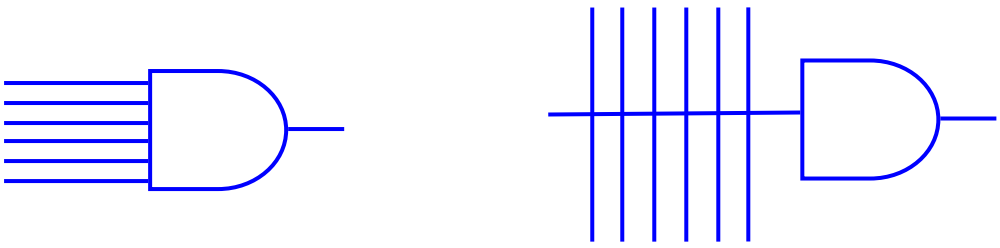


Programmable Logic Array (PLA)

Sometimes, it is not necessary to produce all the minterms of the given input variables because a large number of them are perhaps don't care conditions. In such case we can use a combinational circuit that generates a limited number of product terms and provides an array of OR gates for the outputs. Such a circuit is the programmable logic array.

The logic diagram is for a PLA with three inputs, four product terms and two outputs. The diagram is drawn using the Array Logic graphic symbol.

Array Logic Graphic Symbol



Conventional symbol Array logic symbol