Temperature insensitive current-mode CMOS exponential function generator and its application in variable gain amplifier

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1. Introduction

An exponential function generator produces an output waveform (current/voltage) which is an exponential function of the input waveform (current/voltage). The exponential characteristics can be easily obtained in BJT or BiCMOS technologies using the intrinsic exponential characteristics \((V_C = f(V_B))\) of the bipolar transistors [1]. However, it is not easy to realize such function in CMOS technology because of the inherent square-law or linear characteristics of MOSFET operating in strong inversion region. The widely used technique to implement analog exponential function circuits using MOSFET in strong inversion is based on pseudo-approximations. To mathematically implement the exponential function by this method, different approximations have been already introduced; Taylor series 2nd order [2–5], Taylor series 4th order [6], Pseudo exponential [7], Pseudo–Taylor approximation [8], Modified Pseudo–Taylor approximation [9] and rational function approximation [10].

On the other hand, a MOSFET device biased in weak inversion region is a well-known approach to produce an exponential function due to the exponential relationship between \(I_{DS} \) and \(V_{GS}\) of MOSFET in weak inversion regime; see for example Refs. [11,12,15] and some of the references cited therein. The drain current of MOSFET in weak inversion region is given by

\[
I_{DS} = 2\mu n C_{ox} \frac{W}{L} e^{\frac{(V_{GS}-V_T)}{V_{TH}}} \tag{1}
\]

Although the low \(V_{GS}\) voltage makes this technique efficient in low voltage applications compared with realizations that use MOSFET in strong inversion regime, the exponential relation between \(I_{DS}\) and \(V_{GS}\) suffers from strongly temperature dependency, threshold voltage variation effect, and sensitivity to process parameters variation.

In this paper, a new exponential approximation is proposed. The new approximation demonstrates 96 dB output dynamic range over maximum input range \(-5.75 \leq x \leq 5.75\) while keeping linearity error less than \(\pm 0.5\) dB level. The implemented circuit is designed and simulated using 0.35 \(\mu\) CMOS process.

2. Proposed exponential circuit design

2.1. Design concept

Based on Taylor’s series expansion, the exponential function can be approximated as expressed by Eq. (2):

\[
e^x = 1 + \frac{x}{2!} + \frac{x^3}{3!} + \frac{x^4}{4!} + \cdots + \frac{x^n}{n!} + \cdots \tag{2}
\]

where \(x\) is the independent input variable. For \(-1.2 \leq x \leq 2.0\); the higher order terms in Taylor’s approximation can be neglected and
Eq. (2) can be approximated up to the 4th order with 30 dB linear output range whereas the error in ±0.5 dB level. It implies that large output range requires more terms and consequently more complexity.

The proposed technique in this paper is incorporation of pseudo-exponential, 4th-order and coefficients optimization at the same time to significantly extend the output range without higher terms. The proposed approximation can be expressed as

$$e^x = \frac{e^{x/1.2x}}{e^{-x/1.2x}} = \frac{1 + \sum_{n=0}^{\infty} Y_n x^n / 2^n n!}{1 + \sum_{n=0}^{\infty} (-1)^n Y_n x^n / 2^n n!}$$

(3)
equivalently, the numerator and denominator can be rewritten as illustrated in Eq. (4):

$$e^x = \frac{1 + \sum_{n=0}^{\infty} \left( Y_0 x^n / 2^n n! \right)}{1 + \sum_{n=0}^{\infty} \left( (-1)^n Y_n x^n / 2^n n! \right)}$$

(4)

where $Y_0$, $Y_1$, $Y_2$, $Y_3$ and $Y_4$ are linear polynomial coefficients which introduced to be optimized. The “Linear Least Squares” optimization method in MATLAB tool has been used to compute the optimum values for the coefficients $Y_0$, $Y_1$, $Y_2$, $Y_3$, and $Y_4$ of the polynomials in Eq. (4) that approximate $e^x$ for input range $-5.75 \leq x \leq 5.75$ which result in 96 dB linear output range. It was found that $Y_0 = 0.025$, $Y_1 = 1$, $Y_2 = 3/4$, $Y_3 = 3/8$, and $Y_4 = 3/32$. One of the features of this approximation and the obtained coefficients’ values is that a “perfect square trinomial” form can arise in the numerator and denominator which lead to the following final approximation:

$$e^x = \frac{0.025 + (1 + 0.125)x^4}{0.025 + (1 - 0.125)x^4}$$

(5)

The major difference in the proposed pseudo-exponential rather than conventional approximations is the consideration of the terms $x^2$ and $x^3$ only while the term $x^4$ has been eliminated. These terms can be simply and accurately implemented in the CMOS technology. One squaring unit and two cascaded can provide the terms $x^2$ and $x^3$, respectively. Furthermore, the output range was extended more around three times compared to the conventional 4th order approximation with fewer terms.

Fig. 1 shows the dB-scale of the proposed exponential function approximation given in Eq. (5). Fig. 2 shows a comparison between different approximation techniques reported in the literature and Fig. 3 shows the error in each approximation. Inspection of Figs. 2 and 3 clearly shows that the proposed approximation of Eq. (5) achieves the best output range and maximum normalized input range compared to the other approximations with ±0.5 dB error. Table 1 compares the input and output ranges of different approximations.

2.2. Circuit description

Fig. 4 shows the block diagram of the proposed implementation of the exponential function of Eq. (5). In the following subsections the description of each block will be given and it will be shown that the relationship between the input current $I_\text{in}$ and the output current $I_\text{out}$ will be given by

$$I_\text{out} = I_\text{ref} \frac{I_{\text{num}}}{I_{\text{den}}} = I_\text{ref} \left( I_\text{in} / I_{\text{ref}} \right)$$

(6)

where $I_\text{in}$ and $I_{\text{ref}}$ are reference currents.

2.2.1. Squaring circuit

The circuit diagram of the squaring circuit used in Fig. 4 is shown in the dashed box in Fig. 5 [13]. The aspect ratios of all transistors are listed in Table 2.
Table 1
Performance comparison between different exponential approximations approaches.

<table>
<thead>
<tr>
<th>Approximation</th>
<th>Equation</th>
<th>Input range</th>
<th>Output range (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2nd order taylor series [2–5]</td>
<td>$1 + x + \frac{1}{2}x^2$</td>
<td>$-0.6 \leq x \leq 0.05$</td>
<td>13.3</td>
</tr>
<tr>
<td>4th order taylor series [6]</td>
<td>$1 + x + \frac{1}{2}x^2 + \frac{1}{2}x^4$</td>
<td>$-1.2 \leq x \leq 2.0$</td>
<td>30</td>
</tr>
<tr>
<td>Pseudo exponential [7]</td>
<td>$e^x \approx \frac{1 + 0.5x}{1 + 0.5x}$</td>
<td>$-0.85 \leq x \leq 0.85$</td>
<td>14.8</td>
</tr>
<tr>
<td>Pseudo–Taylor approximation (m = 1) [8]</td>
<td>$e^x = \frac{e^{0.5x}}{m + x}$</td>
<td>$-1.08 \leq x \leq 1.08$</td>
<td>17.8</td>
</tr>
<tr>
<td>Pseudo–Taylor approximation (m = 0.82) [8]</td>
<td>$e^x = \frac{e^{0.5x}}{m + x}$</td>
<td>$-1.63 \leq x \leq 1.63$</td>
<td>27.2</td>
</tr>
<tr>
<td>Modified Pseudo–Taylor approximation [9]</td>
<td>$e^x = \frac{12 + 1}{1 + 0.25x}$</td>
<td>$-3.1 \leq x \leq 3.1$</td>
<td>56</td>
</tr>
<tr>
<td>Rational function approximation [10]</td>
<td>$e^x = \left[\frac{1}{12}\left(1 + 0.25x\right)^2\right]$</td>
<td>$-3.3 \leq x \leq 3.3$</td>
<td>60</td>
</tr>
<tr>
<td>Proposed</td>
<td>$e^x = \left[\frac{1}{12}\left(1 + 0.25x\right)^2\right]$</td>
<td>$-5.75 \leq x \leq 5.75$,</td>
<td>96</td>
</tr>
</tbody>
</table>

Applying translinear loop principle in Fig. 5 for transistors M1–M4 yields

$$V_{g31} + V_{g32} = V_{g33} + V_{g34}$$

(7)

where $V_{g31}$, $V_{g32}$, $V_{g33}$ and $V_{g34}$ are the gate-to-source voltages of transistors M1, M2, M3 and M4, respectively. From Eq. (7), with the four MOSFETs operating in weak inversion, it is easy to show that $I_1 = I_2 = I_3 = I_4 = I_{out}$

$$I_{out} = \frac{I_2}{4I_{ref}}$$

(9)

Eq. (9) represents the current-mode squaring function. The squaring circuit is a key block in the proposed current-mode exponential function generator of Fig. 4.

2.2.2. Current divider

The circuit diagram of one quadrant current-mode divider is shown in the dashed box in Fig. 6 [14]. A single quadrant current divider function is realized using transistors Ma–Md where all transistors are operating in the sub-threshold region. Writing the translinear loop for the transistors in the dashed box gives

$$V_{sga} + V_{sgb} = V_{sgc} + V_{sgd}$$

(10)

with transistors Ma–Md working in the subthreshold region. Eq. (10) yields

$$I_{d}I_{d} = I_{num}I_{den}$$

(11)

If $I_{a} = I_{num}$, $I_{b} = 0.125I_{num}$, $I_{c} = 0.125I_{den}$, and $I_{d} = I_{out}$, then Eq. (11) will become

$$I_{out} = \frac{I_{num}}{I_{den}}$$

(12)

The transistor aspect ratios of Fig. 6 are shown in Table 3. It is worth mentioning here that $(W/L)_h = (1/8)(W/L)_{lh}$ to scale down the currents $I_{num}$ and $I_{den}$ so that transistors Mb and Mc will remain operating in weak inversion. This implies that the aspect ratios of all the transistors involved in the translinear loop must be selected to meet the anticipated dynamic range of the input and output currents.

2.2.3. Bidirectional current mirror (BDCM)

Fig. 7 shows the circuit diagram of the current mirror used. If the input current is $I_1$, then two copies of this current can be obtained at the output, $I_2$ and $-I_2$. The aspect ratios of all the transistors used are listed in Table 4.
2.2.4. Mathematical analysis

With reference to Fig. 4, there are six nodes A–F. Applying KCL at each node and using Eq. (9) yields the following:

\[ I_A = -(8I_{ref} + I_x) = -8I_{ref}(1 + 0.125(l_x/I_{ref})) \]  
(13)

\[ I_B = -(8I_{ref} - I_x) = -8I_{ref}(1 - 0.125(l_x/I_{ref})) \]  
(14)

\[ I_C = \frac{(8I_{ref})^2(1 + 0.125(l_x/I_{ref}))^2}{4I_{ref}} \]  
(15)

\[ I_D = \frac{(8I_{ref})^2(1 - 0.125(l_x/I_{ref}))^2}{4I_{ref}} \]  
(16)

Table 3

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Aspect ratio</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ma, Md</td>
<td>196/1.4</td>
<td>140</td>
</tr>
<tr>
<td>Mb, Mc</td>
<td>175/1.4</td>
<td>125</td>
</tr>
<tr>
<td>Me–Mh</td>
<td>7/7</td>
<td>1</td>
</tr>
<tr>
<td>Mi–Mk</td>
<td>19.6/19.6</td>
<td>1/1</td>
</tr>
<tr>
<td>Mm–Mn</td>
<td>1/1</td>
<td>1/1</td>
</tr>
</tbody>
</table>

Table 4

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Aspect ratio</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mn1–Mn5</td>
<td>1/10</td>
<td>0.1</td>
</tr>
<tr>
<td>Mp1–Mp5</td>
<td>1.7/10</td>
<td>0.17</td>
</tr>
</tbody>
</table>

2.3. Simulation results

The functionality of the proposed exponential circuit was verified by simulation using Tanner tools with 0.35 μm CMOS process technology and supply voltage ±0.75 V. The simulation result is illustrated in Fig. 9 where \( I_{ref} \) equals to 25 nA. Thus the x-axis, 150 nA ≤ \( I_x \) ≤ 150 nA, can be normalized as −6 ≤ \( I_x/I_{ref} \) ≤ 6. The curve of the proposed function is very close to the ideal exponential function, \( I_w e^{l_x/25 \, nA} \), with a high output dynamic range, nearly 96 dB. The error between the proposed function and the ideal exponential function, \( I_w e^{l_x/25 \, nA} \), is limited to ±0.5 dB when −137.5 nA ≤ \( I_x \) ≤ 137.5 nA, as illustrated in Fig. 10.

Simulation of transient response was carried out with sinusoidal input signal of frequency 5 kHz. The results are shown in Fig. 11. Simulation for temperature analysis was carried out. The temperature was varied from −25 °C to +75 °C and the simulation result, shown in Fig. 12, shows that the input–output characteristic is
insensitive to temperature variations. The linearity error remains less than $\pm 1.5 \text{ dB}$ for the full scale of the input current range. The maximum deviation of the output current was about $\pm 1.27 \text{ dB}$ and occurred for the normalized value $I_x/I_{\text{ref}} = 5.25$.

Simulation for power supply variation was also carried out. A 10% variation in the supply voltage at room temperature was used. Simulation results shown in Fig. 13 indicate that the circuit is stable with power supply variations within 10% of the nominal value.

Table 5 summarizes the comparison between the performance of the proposed circuit and recently published works. Inspection of Table 5 clearly shows that the proposed exponential function generator enjoys the largest linear-in-dB range of 96 dB while consuming about 6.13 $\mu$W and is stable over a wider range of temperature variations.

4. Mismatch analysis

Referring to Fig. 4, if there is a mismatch in the current mirror used in mirroring the constant current ($1.6I_{\text{ref}}$), i.e., it is equal to $1.6I_{\text{ref}} + \Delta I_{\text{ref}}$), then Eqs. (19)–(21) can be reevaluated and the output current will be expressed as

$$I_{\text{out}} = I_w \frac{I_{\text{num}}}{I_{\text{den}}} = I_w \left\{ \frac{k + (1 + 0.125(I_x/I_{\text{ref}}))^4}{k + (1 - 0.125(I_x/I_{\text{ref}}))^4} \right\}$$

where $k = 0.025 + (\Delta I_{\text{ref}}/64I_{\text{ref}})$. The simulation result shown in Fig. 14 indicates that the deviation due to 10% mismatch is less than $\pm 0.03\%$.

In real implementation, there are always process variation and mismatch effects. To study such effect, Monte Carlo test
has been carried out for 100 iterations. For 5% variation in the aspect ratios of the core transistors in the squaring loop (M1, M2, M3 and M4), the histogram shown in Fig. 15(a) and (b) indicates that the corresponding maximum variation from the nominal value of the output current is found to be ±1.8 dB for 1.2 normalized input, while the error in −3 dB frequency is 0.02%.

5. Exponential-control VGA

The linear-in-dB variable gain amplifier (VGA) is usually employed in Automatic Gain Control (AGC) loop to increase the signal-to-noise ratio (SNR) in wireless receivers [16], to enhance the system performance regarding the linearity, SNR and power consumption in the global positioning system (GPS) receivers [17], in disk drives [18], in biomedical signal acquisition [19] and direct-conversion receivers [20]. Various approaches to implement VGAs circuits have been reported [16–23] and such circuits can be found in several signal processing applications. Among the most significant demands of VGAs are the wide range of gain variation, low sensitivity against voltage supply variation, small chip size and low power consumption. In the following subsection a description for a new proposed exponential-control VGA, using the exponential function generator described in Fig. 8 will be highlighted.

5.1. Proposed exponential-control VGA

The proposed exponential-control VGA, shown in Fig. 16, was developed based on the new exponential function generator obtained based on the approximation given in Eq. (5) and its CMOS implementation shown in Fig. 8. In Fig. 16 the control signal is applied to the input of the EXPFG cell and the input small signal...
has been added to the DC component in the divider included in EXPFG. Applying the Kirchhoff’s Current Law (KCL) at node Z in Fig. 16 and using Eqs. (24)–(27) yields

Using Eq. (22) the currents \( I_{out,1} \) and \( I_{out,2} \) can be expressed as

\[
I_{out,1} = (I_w + I_{in}) e^{I_{ctrl}/I_{ref}} \tag{24}
\]

\[
I_{out,2} = I_w e^{I_{ctrl}/I_{ref}} \tag{25}
\]

Applying KCL at node \( z \) yields

\[
I_{out} = I_{out,1} - I_{out,2} = (I_w + I_{in}) e^{I_{ctrl}/I_{ref}} - I_w e^{I_{ctrl}/I_{ref}} \tag{26}
\]

or

\[
I_{out} = I_{in} e^{I_{ctrl}/I_{ref}} \tag{27}
\]

Eq. (24) can be rewritten as

\[
A_i = \frac{I_{out}}{I_{in}} = e^{I_{ctrl}/I_{ref}} \tag{28}
\]

where \( A_i \) is the current gain, \( I_{ctrl} \) is the control signal and \( I_{ref} \) is the reference constant current. From Eq. (28), it is obvious that a variable-gain current amplifier can be realized and its gain can be exponentially controlled by the control current \( I_{ctrl} \).

The gain in linear dB scale is calculated as follows:

\[
A_i (dB) = 20 \log_{10}(e^{I_{ctrl}/I_{ref}}) \tag{29}
\]

Table 5
Performance comparison table between different exponential function circuits.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[2]*</th>
<th>[10]</th>
<th>[12]</th>
<th>[15]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage supply</td>
<td>1 V</td>
<td>1.8 V</td>
<td>1.5 V</td>
<td>1.8 V</td>
<td>± 0.75 V</td>
</tr>
<tr>
<td>Process</td>
<td>0.35 μm CMOS</td>
<td>0.18 μm CMOS</td>
<td>0.35 μm CMOS</td>
<td>0.18 μm CMOS</td>
<td>0.35 μm, 2p4m CMOS</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>3.5 μW</td>
<td>NA</td>
<td>400 μW</td>
<td>214 nW</td>
<td>6.13 μW</td>
</tr>
<tr>
<td>Technique</td>
<td>Approximation</td>
<td>Approximation</td>
<td>Exact</td>
<td>Exact</td>
<td>Approximation</td>
</tr>
<tr>
<td>Operation region</td>
<td>Weak inversion</td>
<td>Strong inversion</td>
<td>Weak inversion</td>
<td>Weak inversion</td>
<td>Weak inversion</td>
</tr>
<tr>
<td>Input signal</td>
<td>Current</td>
<td>Current</td>
<td>Voltage</td>
<td>Voltage</td>
<td>Current</td>
</tr>
<tr>
<td>Output signal</td>
<td>Current</td>
<td>Current</td>
<td>Current</td>
<td>Current</td>
<td>Current</td>
</tr>
<tr>
<td>Linear-in-dB range</td>
<td>8.5 dB</td>
<td>58 dB</td>
<td>40 dB</td>
<td>NA</td>
<td>96 dB</td>
</tr>
<tr>
<td>Linearity error</td>
<td>± 0.45 dB</td>
<td>± 0.5 dB</td>
<td>± 0.75 dB</td>
<td>± 0.92 dB</td>
<td>± 0.5 dB</td>
</tr>
<tr>
<td>BW</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>− 10 C: 70 C</td>
</tr>
<tr>
<td>ΔT range</td>
<td>NA</td>
<td>NA</td>
<td>− 3 dB</td>
<td>Dependent</td>
<td>± 1.27 dB</td>
</tr>
<tr>
<td>Error due ΔT</td>
<td>NA</td>
<td>NA</td>
<td>± 10% V</td>
<td>NA</td>
<td>± 10% V</td>
</tr>
<tr>
<td>ΔV range</td>
<td>NA</td>
<td>NA</td>
<td>± 1 dB</td>
<td>NA</td>
<td>± 3.35 dB</td>
</tr>
<tr>
<td>Error due ΔV</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

* Experimental.

Fig. 14. Effect of mismatch in the current mirror.

Fig. 15. (a) Monte Carlo analysis for output current when normalized input = 1.2 and (b) the frequency bandwidth histogram.

Fig. 16. The proposed structure of exponential-control VGA.
Eq. (29) can be rewritten as

$$A_i(\text{dB}) = 8.69 \frac{I_{\text{ctrl}}}{I_{\text{ref}}}$$

Eq. (30) readily shows that the gain in dB scale is linearly proportional to the control signal.

Fig. 17. Simulation results of the proposed exponential-control VGA.

Different gain values effect.

Fig. 18. VGA response with triangular control signal.

Fig. 19. VGA response with sinusoidal control signal.

Fig. 20. Transient analysis of the overall circuit $I_{\text{in}}$ is a 10-kHz sinusoidal signal and $I_{\text{ctrl}}$ is a ramp. $I_{\text{out}}$ is shown to have variable amplitude.

Fig. 21. Load effect figure.
5.2. Simulation results of the proposed VGA

Simulation results are given to verify the functionality of the proposed VGA. Tanner tool is used with standard 0.35 μm CMOS process to simulate the proposed structure of exponential-control VGA in Fig. 16. The DC supply voltage set to ±0.75 V and the current $I_{\text{ref}}$ was set to 25 nA. Fig. 17 shows that the output control range is around 71 dB with ±0.5 dB linearity error. Different values of $I_{\text{ctrl}}$ (−17.33 nA, 0 nA and 17.33 nA) have been used to meet −6 dB, 0 dB and 6 dB gain values, respectively, and as a result the eventual output signal changed accordingly as shown in Fig. 18.

Transient analysis of the overall circuit is shown in Fig. 19; where $I_{\text{ref}}$ is a sinusoidal signal with 10 kHz frequency and 20 nA amplitude and $I_{\text{ctrl}}$ is chosen to be a ramp signal. The figure demonstrates the variable gain effect on the amplitude of the output current.

Simulation was carried out to confirm the functionality of the proposed VGA when 10 kHz sinusoidal input signal and amplitude 20 nA was used. The control signal was a triangular of 200 nA peak-to-peak and a frequency of 1 kHz and 10 kHz sinusoidal with amplitude of 100 nA as shown in Figs. 20 and 21, respectively. When $I_{\text{ctrl}} = 100$ nA the VGA gives highest amplification and when $I_{\text{ctrl}} = −100$ nA it gives highest attenuation.

The effect of the load and different amplitudes has been studied and simulated by sweeping the load from 0 to 10 MΩ when the amplitude is set to 40 nA and the amplitude of the input varies from 10 nA to 50 nA when the load set to be 10 kΩ and results are shown in Figs. 22 and 23, respectively.

AC simulation is given in Fig. 24 with resistive (R) and complex (RC) load effect. If $R = 10$ kΩ while Gain = −6 dB, 0 dB and 6 dB, the corresponding −3 dB frequency is 174 kHz, 242 kHz and 291 kHz, respectively but if a capacitance $C = 50$ pF is added in parallel with $R$, then for Gain=0.5, 1 and 2 the −3 dB frequency is 132 kHz, 170 kHz and 181 kHz, respectively.

Table 6 outlines the most important features of the proposed VGA compared to the prior works. These performance parameters are either better or compare favorably with the reported state-of-the-art VGAs.

### Table 6
Comparison with prior works.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>[20]</th>
<th>[21]</th>
<th>[22]</th>
<th>[23]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process (CMOS) (μm)</td>
<td>0.18</td>
<td>0.5</td>
<td>0.18</td>
<td>0.18</td>
<td>0.35</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>−3 to 45</td>
<td>−26.79 to 23.94</td>
<td>0−95</td>
<td>−10 to 50</td>
<td>−49 to 22</td>
</tr>
<tr>
<td>Stages</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>Voltage supply (V)</td>
<td>1.8</td>
<td>2</td>
<td>1.8</td>
<td>1.8</td>
<td>±0.75</td>
</tr>
<tr>
<td>BW</td>
<td>3 MHz</td>
<td>134 kHz</td>
<td>32 MHz</td>
<td>8 MHz</td>
<td>181 kHz*</td>
</tr>
<tr>
<td>Power consumption</td>
<td>0.549 mW</td>
<td>1.6 μW</td>
<td>6.48 mW</td>
<td>6.7 mW</td>
<td>12.782 μW</td>
</tr>
</tbody>
</table>

* R≈0.5 μs and Gain≈2.
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References


