KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS

Electrical Engineering Department

EE-203 Electronics I: First Semester 2004-2005 (041)

Instructor: Dr. Hussain A. Alzaher — Office Location: 14-272

Office Hours: S.M.W. 9:20-9:50AM & 12:30-1PM — Class Location: 7-127

Text: Microelectronic Circuits, 5^{h} Ed. 1998, by Sedra and Smith, Oxford University Press, Inc.

W	Date	Sections	Topics	Lab./PSPICE
1	Sep 11 – 15	3.1,3.2, 3.3	**Diodes: Chap. 3** Introduction, PN junction, physical operation of diode, diode characteristics, ideal diode	**No Lab.**
2	Sep 18 – 22	3.4, 3.6	Diode Models, diode applications: limiters, Zeners, regulators	**Exp. # 1** Intr. to Lab. Equipment
3	Sep 25 – 29	3.7, 3.8	Analysis of diode circuits, more diode applications: rectifiers	**Exp. # 2** Introduction to PSPICE
4	Oct 2-6	5.1, 5.2, 5.3	**Bipolar Junction Transistors (BJTs) : Chap. 4** Physical operation, types, symbols and conventions, transistors characteristics, active and saturation regions, BJT as a Switch	**Exp. # 3** Diode Applications
5	Oct 9-13	5.4, 5.5, 5.6	DC biasing and analysis of BJT circuits, BJT Small-signal equivalent circuit models.	**Exp. # 4** DC Power Supply
6	Oct 16-20	5.7	Basic single-stage BJT amplifiers: CE, CB and CC	**No Lab**
Sat, Oct 23, Exam I (Tentative class time)				
7	Oct 23-27	4.1, 4.2	**Field-Effect Transistors (FETs): Chap. 5** Physical operation of MOSFET/JFET, terminal characteristics	**Exp. # 5** BJT Characteristics
Tue, Oct 26, Last Day for dropping courses with grade 'W'				
8	Oct 30- Nov 3	4.3, 4.4, 4.5, 4.6	DC analysis of MOSFET/JFET, small signal models	**Exp. # 6** BJT CE Amplifier
Sat, Nov 6- Wed Nov 17 (Ramadan Vacation)				
9	Nov 20- 24	4.7, 4.11	FET amplifiers: CS, CG and CD amplifiers BJT vs MOS amplifiers	**Exp. # 7** MOSFET Amplifiers
10	Nov 27- Dec 1	7.3	**Differential Amplifiers: Chap. 6** BJT Differential amplifier	**Exp. # 8** JFET Characteristics & Application
Wed, Dec 1, Last Day for withdrawal from all courses with grade 'W'				
11	Dec 4- 8	7.1, 7.2	MOS Differential amplifier **BJT Logic Gates: Chap. 14** Digital circuit specifications, noise margins, fan-in, fan-out ,	**Exp.#9** BJT differential amplifier
12	Dec 11- 15	5.10, **Handout**	BJT logic families, TTL Inverter Other TTL circuits (NAND, NOR, …)	**No Lab**
Mon, Dec 13, Exam II (Tentative time : 7:00 – 9:00 pm)				
13	Dec 18- 22	10.2	ECL logic circuits (e.g. NOR/OR) TTL vs. ECL **CMOS Logic Gates: Chap. 13, 14** CMOS logic inverter	**Exp#10** TTL Logic Gates
14	Dec 25- 29	10.3	CMOS logic gates: Analysis and design	**Exp. # 11** CMOS Inverter
Wed, Dec 29, Last Day for withdrawal from all courses with grade 'WP/WF'				
15	Jan 1-3	10.5	transistor sizing, pass transistor logic circuits, BJT vs. MOS Logic: advantage/disadvantages BiCMOS logic circuits	**Lab Final**

Grading: Homework 5%, Quizzes 10%, Participation 5%, Design project 5%, Two Major Exams 25%, Final 30 %, Lab. 20%.

Absence: **University Rule: 6** unexcused absences → Warning; **9** unexcused absences → **DN**

Note : Thursday, Sep 23 is normal Tue Class

Thursday, Sep 30 is normal Wed Class