DIGITAL LOGIC GATES

OBJECTIVE:

- To study the basic logic gates: AND, OR, INVERT, NAND, and NOR.
- To study the representation of these functions by truth tables, logic diagrams and Boolean algebra.
- To observe the pulse response of logic gates.
- To measure the propagation delay of logic gates.

APPARATUS:

- IC Type 7400 Quadruple 2-input NAND gates
- IC Type 7402 Quadruple 2-input NOR gates
- IC Type 7404 Hex Inverters
- IC Type 7408 Quadruple 2-input AND gates
- IC Type 7432 Quadruple 2-input OR gates
- IC Type 7486 Quadruple 2-input XOR gate
- IC Type 7493 4-bit ripple counter
- Digi-Designer Logic Board
- Dual-trace oscilloscope

THEORY:

AND A multi-input circuit in which the output is 1 only if all inputs are 1.The symbolic representation of the AND gate is shown in Fig. 1a.

OR A multi-input circuit in which the output is 1 when any input is 1. The symbolic representation of the OR gate is shown in Fig. 1b.

INVERT The output is 0 when the input is 1, and the output is 1 when the input is 0. The symbolic representation of an inverter is shown in Fig. 1c.

NAND AND followed by INVERT. The symbolic representation of the NAND gate is shown in Fig 1d.

NOR OR followed by INVERT as shown in Fig 1e.

EX-OR The output of the Exclusive –OR gate, is 0 when it's two inputs are the same and it's output is 1 when its two inputs are different.

Truth Table Representation of the output logic levels of a logic circuit for every possible combination of levels of the inputs. This is best done by means of a systematic tabulation.

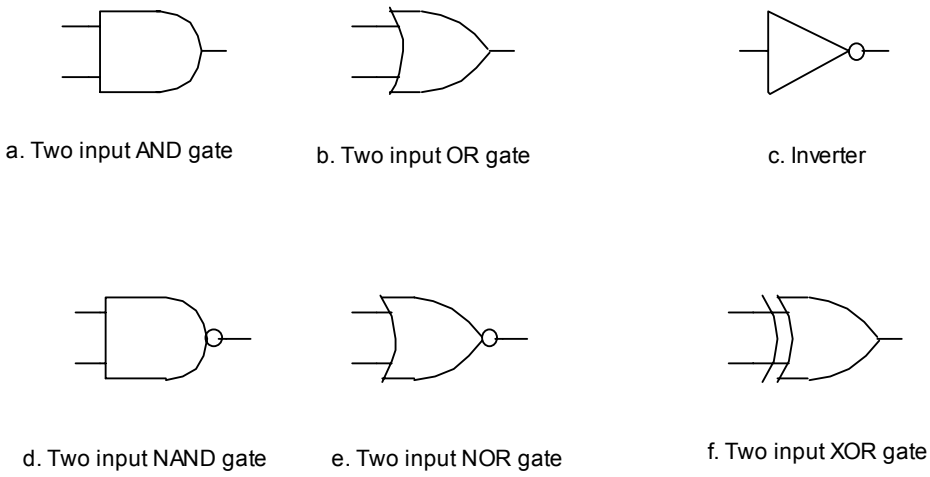


Fig.1 Symbols for digital logic gates

Part 1: Logic Functions

I. AND, OR, NAND, and NOR gates.

1. Use one gate for each IC 7400 (NAND), 7402 (NOR), 7408 (AND), 7432 (OR), 7486 (XOR). Each has input pins, 1 and 2, and output pin 3.

2. Connect pin 1 to switch S1-1, pin 2 to switch S1-2, and pin 3 to LED-1 for every gate as shown in Fig 2 as an example for the NAND gate.

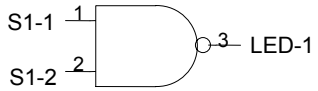


Fig.2 Two input NAND gate

3. Using logic switches S1-1 and S-2, apply the logic levels 0 and 1 to gate inputs (pin 1, pin 2), in the sequence shown in table 1. Record the output logic levels (see lamp LED-1) in table 1. Repeat the recordings for each gate.

Remember: Lamp ON = Logic 1, (High)
Lamp OFF = Logic 0 (Low)

Table 1

Pin 1	Pin 2	Pin 3

4. Use an inverter gate from IC 7404 whose input pin is pin 1 and whose output pin is pin 2.

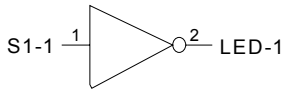


Fig.3 Inverter gate

5. Using logic switches S1-1, apply the logic levels 0 and 1 in the sequence shown in table 2. Record the output logic levels in table 2

Table 2.

Pin 1	Pin 2
0	
1	

Part-2: Response of Logic Gates:

Connect the circuits of figures 4 and 5 and write the corresponding truth tables 3 and 4, respectively.

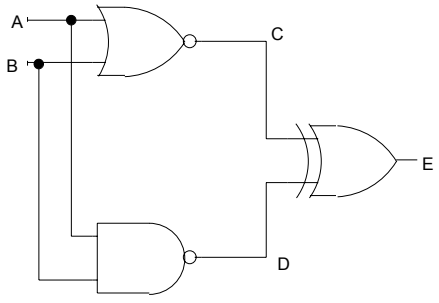


Fig. 4

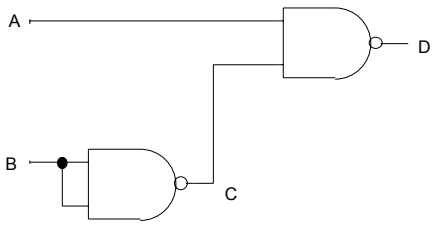


Fig. 5

Table 3.

A	B	C	D	E
0	0			
0	1			
1	0			
1	1			

Table 4.

A	B	C	D
0	0		
0	1		
1	0		
1	1		

Part-3: Propagation Delay in Logic Gates:

Connect all inverters inside two 7404 Ics in cascade. The output will be the same as the input except that it will be delayed by the time it takes the signal to propagate through all six inverters. Set S2 to 100 kHz and apply clock pulses to the input of the first inverter (connect pin 1 to j14) record the wave forms and determine the time delay from the input to the sixth inverter. This is done with a dual trace oscilloscope by applying the input clock pulses to one of the channels and the output of the sixth inverter to the second channel and measuring the delay between the two signals as shown in Fig 6. By using measured delay between two signals calculate the propagation delay for each inverter gate.

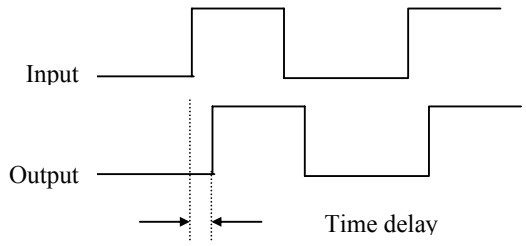
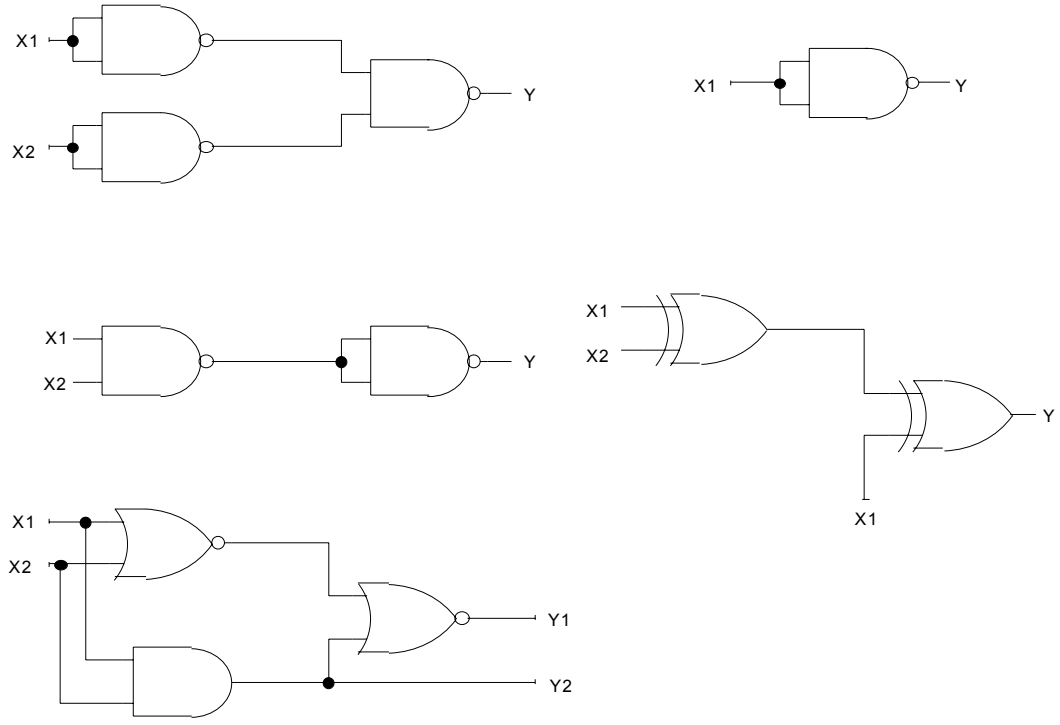


Fig. 6 Propagation delay

Part 4: Review Questions:

1. Write a truth table for each circuit. Derive Boolean expressions for all outputs.



2. A burglar alarm for a car has a normally low switch on each of four doors. If any door is opened the output of that switch goes HIGH. The alarm is set off with an active-LOW output signal. What type of gate will provide this logic? Support your answer with an explanation.