Resumé of

Professor Sadiq M. Sait, Ph.D

Department of Computer Engineering
College of Computer Sciences and Engineering
King Fahd University of Petroleum and Minerals
KFUPM # 673, Dhahran 31261, Saudi Arabian
e-mail: sadiq@ccse.kfupm.edu.sa

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Bio-Data

Professor **Sadiq M. Sait**, Ph.D.

Work Address
King Fahd University of Petroleum and Minerals
KFUPM # 673
DHAHRAN-31261
Saudi Arabia
(03)-860-2217 (Off)
Fax:(03)-860-3059 (Attn: Professor **Sadiq M. Sait**, COE Dept)

Home Address
KFUPM Al-Nakheel Compound
House Number 6526
Dhahran-31261
Saudi Arabia
Tel:(03)-860-6665 (Res)

Family Status : Married with three children.
Date of Birth : October 28, 1957
Nationality : Saudi Arabian

Education

Ph.D. in ELECTRICAL ENGINEERING, (Computer Science Minor), King Fahd University of Petroleum and Minerals (KFUPM), November 1986, (GPA $\frac{4.0}{4.0}$). Thesis title: 'VLSI Mask Generation from Register Transfer Level Descriptions: An Automated Approach'.

M.S. in ELECTRICAL ENGINEERING, King Fahd University of Petroleum and Minerals (KFUPM), August 1983, (GPA $\frac{4.0}{4.0}$). Thesis title: 'Hardware Design and Software Development for a Microprocessor Based Application System'.

B.E. in ELECTRONICS ENGINEERING, Bangalore University, India, 1981, (Ranked 2^{nd} in the Entire University).

Employment History

Chairman, since 2000, Department of Computer Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Professor, since 1998, Department of Computer Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Served as Summer Coordinator, College of Computer Sciences & Engineering, June 2000–August 2000, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Associate Professor, 1992–1998, Department of Computer Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Summer Coordinator, July 1993–September 1993, Department of Computer Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Assistant Professor, 1987–1992, Department of Computer Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Lecturer, 1983–1986, Department of Electrical Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Research Assistant, 1981–1983, Department of Electrical Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia.

Academic Background

Computer Architecture, VLSI Design, Switching Theory, Micro-electronics, Hardware Description Languages, Logic Synthesis and Digital Design Automation.

Research Interest

VLSI Physical Design Automation, Microelectronics, High-Level Synthesis, Computer Architecture, Stochastic Search Algorithms.

Membership of Professional Societies

1. IEEE & IEEE Computer Society
2. Saudi Arabian Computer Society.

Academic Honors

1. Invited **Keynote Speaker** at the **International Conference on Microelectronics**, ICM'95, Malaysia, December 1995.
2. Nominee for the **'Distinguished Teacher Award'** *three* times, and received the award *once* (from 'King Fahd University of Petroleum and Minerals'), in 1995.
3. Received the **'Distinguished Researcher Award'** *three* times from 'King Fahd University of Petroleum and Minerals', in 1990, 1994, and 1999.
4. Nominated by the Department of Computer Engineering for the **'Best Advisor Award'** *two* times.
5. **Editor** of *'Arabian Journal for Science and Engineering (AJSE)'* for Computer Science and Engineering 1992-present.
6. AJSE *'Arabian Journal for Science and Engineering'* Editor for the special issue on on Microelectronics.
7. Guest Editor for a special issue on 'Hardware Description Languages', for *International Journal of Computer-Aided VLSI Design,* 1989.
8. Member of the Editorial Board of *International Journal of Computer Aided VLSI Design,* 1987-1992.
9. Nominated to appear in **Marquis Who's Who in the World** (to be listed in 1996 Edition).
10. Awarded the **'Distinguished Teacher and Advisor Award'** (from 'King Fahd University of Petroleum and Minerals'), in 2000.

Research

Area of Work and Projects Completed

With advances in VLSI Design Automation (DA) the Microelectronics industry is undergoing a major revolution. The future of Microelectronics is totally linked to innovation and research in Design Automation (DA) of VLSI Synthesis Systems. Considerable research work is underway at KFUPM in this field. An example of this is the project undertaken to explore solutions to problems of speed performance in VLSI circuits (KFUPM Research committee funded, Project # COE/DESIGN/162, Co-investigator).

On a related track, I (along with Dr. M. S. Benten, who joined my group in 1991) completed the integration of a state-of-the-art VLSI Design Automation System which is being used to design VLSI chips in Saudi Arabia (KACST funded project, Project # AR 11-21, Principal Investigator).

High-level synthesis of digital systems is another major research area (related to VLSI DA) that has also found support at the university. Two high-level synthesis (HLS) systems have been designed and implemented. Four MS theses, four journal publications, and eight conference papers have resulted from this work (KFUPM Research committee funded Project # COE/DESIGN/145, Co-investigator).

The experience gained on these projects and research work has culminated in the writing of the text book entitled '**VLSI Design Automation: Theory and Practice**', which was published by McGraw-Hill Book Co., Europe in January 1995. (KFUPM Research committee funded Project # COE/AUTOMATION/163, Principal investigator).

Excellent has been the grading received for each of the above works. Be it the different projects and their reports or the book published. The book received ten reviews (3 from Prentice Hall International, 3 from Mc-Graw Hill Book Co., Europe, and 4 from KFUPM Research Committee,) all of which were Excellent. The book is also co-published by **IEEE Press**, U.S.A. Over 2700 copies were sold in the first 12 months.

In the following paragraphs I will elaborate more on my main contributions to the field of scientific literature.

I made contributions to the scientific literature in two main areas:

- *VLSI Synthesis*; and
- *VLSI Physical Design Automation.*

I will start first by summarizing my contribution to the area of VLSI synthesis. My Ph.D dissertation was in the area of synthesis of VLSI layouts from hardware description languages (HDLs). I investigated and developed a silicon compiler that takes as input descriptions of digital systems in AHPL (an HDL) and produces VLSI layouts completely automatically. This silicon compiler now has evolved into a complete design automation (DA) system and is operational. It is constantly maintained and upgraded by integrating new public domain tools (the work of enhancing the DA system was supported by KACST under project # AR 11-21, and by KFUPM).

The above KACST funded project also helped in establishing a complete DA laboratory which currently houses SunWorkstations and PCs, which run CAD/DA tools. The CAD/DA tools available include both, those developed in-house, and those obtained from other universities and industries. Examples are OctTools, Magic, OASIS, Alliance, AMICAL, VHDL Tools, etc. The lab is used in teaching undergraduate and graduate courses and for MSc/Senior year projects by the COE and EE departments.

The DA system has been used to design VLSI layouts that have been successfully fabricated in the US (Orbit Semiconductors, California) and France (Grenoble). All chips fabricated thus far have worked as per specifications. For publications that resulted from my Ph.D dissertation work, and the work that followed as a result of KACST funding please see the following: for journal publications see Section , papers # 1, 5, 7, 10, 12 and 19. And for publications in conference proceeding see Section , papers # 1, 2, 3, 6, 9, 19, 20, 22, 1, 2, 3, 4, 6, 7, and 8.

I have been constantly upgrading and improving the existing DA system (UAHPL DASys) at KFUPM. In 1987 I was invited to contribute two chapters to an edited book by Dr. George. Zobrist, Professor of Computer Science, University of Missouri, Rolla. The book was published by Ablex Corporation, who periodically produce a series of edited books on VLSI. The titles of chapters are:

- M. Masud and **Sadiq M. Sait** 'UAHPL Silicon Compiler—From RTL Specifications to Custom Layouts: Part-1: The Language and Its Compiler', *Progress In Computer Aided VLSI Design,* Ablex Publishing Corporation, New Jersey, 1990.
- **Sadiq M. Sait** and M. Masud. 'UAHPL Silicon Compiler—From RTL Specifications to Custom Layouts: Part-2: Automatic Generation of MOS Layouts', *Progress In Computer Aided VLSI Design,* Ablex Publishing Corporation, New Jersey, 1990.

Researchers from the US and Europe who visited KFUPM during the International Conference on Microelectronics (December 1993) were very impressed by the quality of our research work, and the design automation research laboratory we established.

Changes in technology also brought about changes in design issues. Systems synthesized automatically had to be performance driven (timing, power, etc.,). In 1990, Dr. H. Youssef, also of COE department teamed up with us (Dr. Benten and myself) in order to work on timing aspects of VLSI physical design. We completed work on a KFUPM funded project (# COE/VLSIDESIGN/162). All reports have been submitted. The project targeted the development of new approaches to solve timing problems in VLSI design. The project attracted several MS students (see Section), which are listed below:

1. Khaled Nassar implemented a timing-driven placement program using the genetic algorithm, and graduated in June 1994.

2. Khaled Al-Farrah implemented several timing prediction algorithms as well as a timing driven floorplanning program using the force-directed approach, and defended his thesis in December 1994.

3. Shahid Khan implemented a timing driven floorplanning program using the genetic approach, and defended his thesis in December 1994.

4. Hazem Abu-Saleh upgraded an existing integrated placement and routing system by making the placement step driven by the routing as well as the timing criteria. He defended his thesis in Spring 1995.

5. Finally, Amir Hashmi (from Information and Computer Sciences Department) developed a timing-driven global routing algorithm for standard cell design. He defended his thesis in Spring 1995.

For journal publications authored this project see Section , papers # 25, and 29. And for publications in conference proceeding see Section , papers # 28, 29, 31, and 32.

Dr. Benten, Dr. Youssef, and I also completed a three year KFUPM project (# COE/DESIGN/145) related to high-level synthesis of digital systems. This project targeted the development of an integrated system for high-level silicon compilation. Two HLS systems were developed. One that synthesizes VLSI layouts from hardware models in C-programming language. The other translates models in *bc* language (Unix utility) to masks for layouts. The project generated four journal publications and 8 conference papers.

Also four MS theses were performed on the project, which are:

1. Hasan Sukhni implemented a C-based high-level synthesis system, and graduated in January 1994.

2. Abdul-Aziz Al-Mulhem implemented a *bc*-based high-level synthesis system, and graduated in June 1994.

3. Essam Hubbi performed an extensive survey of high-level synthesis systems and developed a new intermediate form representation. He graduated in December 1994.

4. Shahid Ali investigated the use of stochastic iterative techniques such as the Genetic Algorithm and Tabu Search to solve the scheduling and allocation problems in High level synthesis. He completed his work in Spring 1994.

For journal publications from this work please see Section , papers # 15, 16, 17, 23. And for conference publications that resulted from this work please see Section , papers # 19, 24, 25, 26, 27, 34, 7, and 9.

My other project related to the same area (VLSI synthesis) has been the work on back-end design of a system to support automatic layout generation from formal hardware models in algorithmic specific language (ASL). For journal publication from this work please see Section , paper # 22. And for conference publications from this work please see Section , papers # 21 and 23.

Finally, for my work in the area of Computer Architecture, and Architectures for VLSI, please see Section , papers # 2, 3, 4, 6, 8, 9, 11, 13, 14, 18, 20, and 21.

My second major contribution to scientific literature in my area of specialization is the book entitled *VLSI Physical Design Automation: Theory and Practice*. The book was published by McGraw-Hill (see attached McGraw-Hill advertisement flyer). The book has been reviewed and praised by several experts in the field. The book was also reviewed by IEEE and was co-published by IEEE Press at the same time as McGraw-Hill. Several universities have either pledged to adopt or adopted the book; University of Minnesota, University of Arizona, and National Technical University of Taiwan, University of Helsinki, to name a few. Reviews of the book were all excellent and over 2700 copies have been sold in the first twelve months since its release. Below, I quote some of the reviews.

- "*This book will be a must reading for the next generation of CAD tool developers...it should become a resource for any course on VLSI design.*" **Dr. Frederick J. Hill, Professor, University of Arizona, USA**.
- "*I found it well written. In my opinion it will better serve needs of teaching than any existing book on this subject...If published I will use it as a text for the next year course*". **Dr. Eugene Shragowitz, Professor, University of Minnesota, USA**.
- "*I find the book very informative and well written and I will probably use it next time I'll teach the course (next fall)... Nice is a mixture of different techniques...Nice examples and exercises...Overall a very useful book which I am very happy to have in my possession*". **Dr. Maciej Ciesielski, Associate Professor, University of Massachusetts at Amherst, USA**.
- "*I cannot overpraise the job you have done. This is an immense improvement on anything published earlier with which I am familiar. The quality of preparation, discussion, depth of coverage, completeness of bibliography, inclusion of problems, examples, figures, etc., is everything I could wish for. I predict immediate success; you'd better start planning your second edition. I wish that the book will achieve the attention it richly deserves*".

Dr. Douglas Reeves, Associate Professor, North Carolina State University, USA.

- "*It is competitive with other books on the market since* **'Preas and Lorenzetti's'** *book is obsolete and Sherwani's and Lengauer's books are appealing only to theoreticians. The book will be the obvious choice of faculty teaching Physical CAD...This book would be an excellent reference for VLSI design...Very good writing, excellent coverage, right kind of textbook. The book may become standard text for teaching Physical Design CAD. The best text, so far (I am an expert, I even wrote a chapter in* **Preas and Lorenzetti's** *book)*". **Anonymous reviewer of IEEE.**

We recently completed the authoring of our new book entitled *"Iterative Computer Algorithms with Applications in Engineering:i Solving Combinatorial Optimization Problems"*. December 1999, IEEE Computer Society Press, California.

Publications in Refereed Journals

1. M. Masud and **Sadiq M. Sait**. 'Universal AHPL-A Language For VLSI Design Automation'. *IEEE Circuits and Devices Magazine,* September 1986, pp 8–14.
2. **Sadiq M. Sait** and M. A. Kulaib. 'A CMOS Cell for Parallelly Loadable Counters'. *International Journal of Electronics*, Vol. 62, No.6, 1987, pp 867–871.
3. A. A. Soomro, M. Rahman, and **Sadiq M. Sait**. 'A General Real-Time Decoder Based on AMD2900 Devices'. *Journal of Microprocessing and Microprogramming,* December 1987, pp 97–113.
4. A. A. Soomro, **Sadiq M. Sait** and M. Rahman. 'A Bit-Slice Micro-processor Based Decoder'. *Journal of Microprocessors and Microsystems,* December 1987, pp 527–534.
5. **Sadiq M. Sait**, A. Y. Yaagoub, and M. Masud. 'A CAD Tool for the Automatic Generation of Microprograms for Systems Modeled in UAHPL'. *Journal of Microprocessors and Microsystems,* October 1988, pp 463–470.
6. M. A. Kulaib, G. F. Beckhoff, and **Sadiq M. Sait**. 'Design of a Programmable Length Memory and its Controller'. *International Journal of Electronics*, Vol 65, No.2, November 1988, pp 923–932.
7. **Sadiq M. Sait** and F. A. Al-Khulaiwi. 'Automatic Weinberger Synthesis from a UAHPL Description'. *International Journal of Electronics*, Vol-69, No.2, 1990, pp 211–224.

8. **Sadiq M. Sait** and M. A. Al-Rashed. 'An Efficient Algorithm for Weinberger Array Folding'. *International Journal of Electronics*, Vol-69, No.4, 1990, pp 509–518.

9. **Sadiq M. Sait** and A. H. El-Maleh. 'A State Machine Synthesizer with Weinberger Arrays'. *International Journal of Electronics*, 1991, Vol 71, No.1, pp 1–12.

10. **Sadiq M. Sait**. 'Integrating UAHPL-DA System with VLSI Design Tools to Support VLSI DA Courses'. *IEEE Transactions on Education*, Vol 35, No.4, November 1992, pp 312–320.

11. **Sadiq M. Sait**. 'An Architecture to Store Path History in a Trellis and its Application to the Viterbi Algorithm'. *International Journal of Electronics*, 1992, Vol 72, No.1, pp 11–19.

12. J. Yazdani, M. Masud and **Sadiq M. Sait**. 'PCB Layout Generation from RTL Specifications'. *International Journal of Electronics*, 1992, Vol 72, No.1, pp 1–10.

13. **Sadiq M. Sait** and M. S. K. Tanvir. 'VLSI Layout Generation of a Programmable CRC Chip'. *IEEE Transactions on Consumer Electronics,* November 1993, Vol 39, No.4, pp 911–916.

14. M. S. T. Benten and **Sadiq M. Sait**. 'GAP: A Genetic Algorithm Approach to Optimize 2-bit Decoder PLAs'. *International Journal of Electronics*, 1994, Vol 76, No.1, pp 99–106.

15. M. S. T. Benten, **Sadiq M. Sait**, A. S. Al-Mulhem, and H. Youssef. 'RTL Structural Synthesis from Behavioral Descriptions in a Unix Environment'. *Arabian Journal for Science and Engineering*, 19:4B, October 1994, pp 783–803.

16. **Sadiq M. Sait**, M. S. T. Benten, H. Youssef, and F. Soleja. 'Automated VHDL Composition from AHPL'. *Arabian Journal for Science and Engineering,* 19:4B, October 1994, pp 771–782.

17. M. S. T. Benten and **Sadiq M. Sait**. 'Genetic scheduling of task graphs'. *International Journal of Electronics*, 1994. Vol 77, No.4, pp 401–415.

18. **Sadiq M. Sait** and W. Hasan. 'Hardware Design and VLSI implementation of a Byte-Wise CRC Generator Chip'. *IEEE Transactions on Consumer Electronics,* Vol 41, No.1, February 1995, pp 195–200.

19. **Sadiq M. Sait**, M. S. T Benten, and A. M. T Khan. 'ASIC Design with UAHPL'. *IEEE Circuits and Devices Magazine,* March 1995, pp 14–24.

20. **Sadiq M. Sait** and A. A. Khalid. 'VLSI Design and Implementation of Systolic Queues'. *Journal of Microprocessors and Microsystems*, April 1995, Vol 19, No.3, pp 139–146.

21. H. M. Alnuweiri and **Sadiq M. Sait**. 'Efficient Network Folding Techniques for Routing Permutations in VLSI'. *IEEE Transactions on Very Large Scale Integrated (VLSI) Systems,* June 1995, pp 254–263.

22. **Sadiq M. Sait**, K. Elleithy and M. Hasan. 'Formal Synthesis of VLSI Layouts from Algorithmic Specifications'. *International Journal of Computer Systems: Science and Engineering*, UK, Vol 11, Number 2, March 1996, pp 67-81. 21 and 23).

23. H. Youssef, **Sadiq M. Sait**, A. S. Al-Mulhem, and M. S. T. Benten. 'High-level Synthesis from Purely Behavioral Descriptions'. *International Journal of Computer Systems: Science and Engineering*, UK, Vol 11, Number 5, 1996. September 1996, pp 125-139.

24. **Sadiq M. Sait**, S. Ali, and M. S. T Benten. 'Scheduling and Allocation in High-level Synthesis using Stochastic Techniques'. *Microelectronics Journal*, Elsevier Science Ltd, North Holland, Vol. 27, No. 8, October 1996, pp 693-712.

25. **Sadiq M. Sait** and H. Youssef. 'Timing Influenced General Cell Genetic Floorplanner', *Microelectronics Journal*, Elsevier Science Ltd, North Holland, Vol. 28, No. 8, March 1997, pp 151-166.

26. **Sadiq M. Sait**, A. A. Farooqui, G. F. Beckhoff. 'The Architecture of a Highly Reconfigurable RISC Data Flow Array (DF-RISC-A) Processor'. *International Journal of Electronics*, Vol. 83, No.4, August 1997. pp 493-518.

27. **Sadiq M. Sait** and Talal Maghrabi. 'Component Selection and Pipelining using Stochastic Evolution Algorithm'. (Manuscript Submitted) Journal of Computers & Electrical Engineering.

28. **Sadiq M. Sait** and Habib Youssef. 'CMOS/BiCMOS mixed design using Tabu Search'. IEE Electronics Letters, Vol. 34, No. 14, 1998, pp 1395-1396.

29. H. Youssef, **Sadiq M. Sait**, and K. Al-Farra. 'Timing Influenced Constraint Graph Based Force-Directed Floorplanning'. Manuscript **accepted** by *INTEGRATION, the VLSI Journal*, 1999. (Conference version already published, see Section , paper # 31).

30. **Sadiq M. Sait**, A. A. Farooqui, G. F. Beckhoff. 'A Novel Technique for Fast Multiplication', *International Journal of Electronics*, Vol 86, No.1, pp 67–77, January 1999.

31. **Sadiq M. Sait**, H. Youssef, K. W. Nassar, and M. S. T. Benten. Timing Driven Genetic Placement', *International Journal of Computer Systems: Science and Engineering*, Vol 14 No 1 January 1999, pp 3–14.

32. H. Youssef and **Sadiq M. Sait**. 'Timing Driven Global Routing for Standard Cell VLSI Design', *International Journal of Computer Systems: Science and Engineering*, Vol 14, No 3, May 1999, pp 175–186.

33. H. Youssef, **Sadiq M. Sait** and Hakim Adiche. 'Evolutionary Algorithms, Simulated Annealing, and Tabu Search: A Comparative Study,' *Engineering Applications of Artificial Intelligence*, IFAC, Pergamon, Vol 14, No 2, 2001. pp 167–181.

34. Habib Youssef, **Sadiq M. Sait**, E. Shragowitz, and H. Adiche. "Fuzzy Genetic Algorithm for Floorplanning", *Engineering Intelligent Systems*, CRL Publishing Ltd, UK, Vol 8, No. 3, September 2000, pp 145-153.

35. Habib Youssef, **Sadiq M. Sait**, and Ali Hussain. "Fuzzy Simulated Evolution Algorithm for VLSI Placement", accepted for publication in the *International Journal on Applied Intelligence*, Special issue on Applied Metaheuristics, Accepted, (to appear in June 2002).

36. Hasan Cam, Mostafa Abd-El-Barr, and **Sadiq M. Sait**. 'Design and Analysis of a High-Performance Hardware-Efficient Memory Allocation Technique'. The Journal of Systems and Software, June 2000 (Submitted).

37. **Sadiq M. Sait**, H. Youssef, H. Barada, and Ahmed Al-Yamani. "A Parallel Tabu Search Algorithm for VLSI Standard-Cell Placement", Journal of Heuristics, Special Issue on Parallel Metaheuristics, (Accepted, to appear in June 2002).

38. H. Youssef, Abdulaziz Al-Mulhem, **Sadiq M. Sait**, M. Atif Khan. "QoS-Driven Multicast Tree Generation Using Tabu Search", The Computer Communications Journal on Advances in Performance Evaluation of Computer and Telecommunications Networking (Special Issue). Elsevier Science Ltd, May 2002 (to appear).

39. Salman A. Khan, Sadiq M. Sait, Habib Youssef. "Topology Design of Switched Enterprise Networks Using Fuzzy Simulated Evolution Algorithm", Engineering Applications of Artificial Intelligence Elsevier Science Ltd, March 2002 (Accepted).

40. Sadiq M. Sait and Munir M. Zahra. "Tabu Search Based Circuit Optimization", Engineering Applications of Artificial Intelligence Elsevier Science Ltd, February 2002 (Accepted).

Summary: Authored 40 journal papers, of these 38 have been accepted/published. I am the principal/single author in 23 of these, and the second author in 15.

Book Chapters & Books (Authored and Edited)

1. **Sadiq M. Sait** and H. Youssef. Book Chapter entitled: *Modern Iterative Algorithms and their Applications in Computer Engineering*, in **The Computer Engineering Handbook**, December 2001 (accepted for inclusion), Editor Vojin Oklobdzija, CRC Press, Boca Raton, Florida, USA.

2. **Sadiq M. Sait** and H. Youssef. *Iterative Computer Algorithms with Applications in Engineering: Solving Combinatorial Optimization Problems.* December 1999, IEEE Computer Society Press, California.

3. **Sadiq M. Sait** and H. Youssef. *VLSI Physical Design Automation: Theory and Practice*, McGraw-Hill Book Co., Europe, December 1994. Also Co-published by **IEEE Press**, USA, January 1995 (Hard bound edition).

4. M. S. T. Benten, **Sadiq M. Sait**, Abdul Raouf, and Samir H.Abdul-Jauwad. **Editors**. 'Advances in Microelectronics. Proceedings of the Fifth International Conference on Microelectronics', Dhahran. KFUPM Press, December 1993.

5. M. Masud and **Sadiq M. Sait** 'UAHPL Silicon Compiler—From RTL Specifications to Custom Layouts: Part-1: The Language and Its Compiler', *Progress In Computer Aided VLSI Design,* Ablex Publishing Corporation, New Jersey, 1990, pp 1–30.

6. **Sadiq M. Sait** and M. Masud. 'UAHPL Silicon Compiler—From RTL Specifications to Custom Layouts: Part-2: Automatic Generation of MOS Layouts', *Progress In Computer Aided VLSI Design,* Ablex Publishing Corporation, New Jersey, 1990, pp 31–64.

Publications in IEEE and International Refereed Conferences

1. **Sadiq M. Sait**. 'A General Cell Placement Procedure for UAHPL Based DA System'. *IEEE Proceedings of* **CompEuro'87,** Hamburg, May 1987, pp 513-514.

2. **Sadiq M. Sait** and M. Masud. 'CAD of Custom VLSI Layouts from RTL Specifications'. *30th Midwest Symposium on Circuits and Systems,* August 1987, Syracuse, New York, pp 554-558.

3. **Sadiq M. Sait**, M. Masud, and G. F. Beckhoff. 'Heuristics for Automatic Routing of Cells Placed by UAHPL Silicon Compiler'. *Second International Conference on Microelectronics and Microcomputers,* Menouf, Egypt, December 1987.

4. M. A. Kulaib, G. F. Beckhoff, and **Sadiq M. Sait**. 'CMOS Programmable Length First-In, First-Out Memory'. *Second International Conference on Micro-Electronics and Micro-computers,* Menouf, Egypt, December 1987.

5. **Sadiq M. Sait**, A. F. Damati, and M. Rahman. 'Systolic Architecture Design for Decoding Convolutional Codes using Viterbi Algorithm'. *Proceedings of International Conference on Mini and Microcomputers and Their Applications*, **MIMI'88**, Barcelona, Spain, June 1988, pp 526–529.

6. M. Masud, **Sadiq M. Sait**, and A. Y. Yaagoub. 'Automatic Generation of Microprograms for Systems Modeled in RTL'. *Proceedings of International Conference on Mini and Microcomputers and Their Applications,* **MIMI'88**, Barcelona, Spain, June 1988, pp 150–153.

7. M. Atiquzzaman and **Sadiq M. Sait**. 'A New Data Loading Technique in Multiprocessor Systems for Image Processing'. *Proceedings of International Conference on Mini and Microcomputers and Their Applications*, **MIMI'88**, Barcelona, Spain, June 1988, pp 457–460.

8. **Sadiq M. Sait**, A. F. Damati, and M. Rahman. 'A New Architecture for Viterbi Decoding and Its CMOS VLSI Implementation'. *31st Midwest Symposium on Circuits and Systems,* Missouri-Rolla, August 1988.

9. **Sadiq M. Sait** and M. Masud. 'Interfacing UAHPL DA System to Silicon Foundry'. *First International Conference on Micro-Electronics*, **ICM'88**, Algiers, November 1988.

10. **Sadiq M. Sait**, A. F. Damati, and M. Rahman. 'A Systolic Algorithm for VLSI Design of a $\frac{1}{n}$ Rate Viterbi Decoder'. *IEEE* **Melecon'89,** April 1989, Portugal.

11. M. Masud, J. Yazdani, and **Sadiq M. Sait**. 'Automatic Generation of PCB Layouts from Register Transfer Level Specifications'. (Accepted) *1989 International Symposium on Circuits and Systems.* China.

12. A. H. El-Maleh and **Sadiq M. Sait**. 'A State Machine Synthesizer with Weinberger Arrays'. *The IEEE Pacific RIM Conference,* Victoria, Canada, 1991.

13. H. Essam, **Sadiq M. Sait** and M. S. T. Benten. 'From Digital System Models in UAHPL to Layouts using ULMs'. (Accepted by) *First Great Lakes Symposium on VLSI*, **GLSVLSI'91**, Michigan, March 1991.

14. M. S. T. Benten and **Sadiq M. Sait**. 'Automatic Implementation of Data Link Controllers from High Level Language Descriptions of Protocols'. (Accepted by) *First Great Lakes Symposium on VLSI,* **GLSVLSI'91**, Michigan, March 1991.

15. A. M. T. Khan, **Sadiq M. Sait** and G. F. Beckhoff. 'VLSI Implementation of Controllers for Communication Protocols from their Petri Net Models'. *IEEE International Symposium on Circuits and Systems,* California, May, 1992.

16. A. M. T. Khan, **Sadiq M. Sait** and G. F. Beckhoff. 'High Level Synthesis of Controllers for Communication Protocols'. *Second Great Lakes Symposium on VLSI,* **GLSVLSI'92**, Kalamazoo, February, 1992, pp 114-121..

17. **Sadiq M. Sait**. 'UAHPL-DA System and VLSI Design Tools to Support VLSI DA Courses,' *SUNY Conference on Educational Technology*, SUNY College, Oneonta, May 27-28, 1992.

18. H. Al-Nuweiri, **Sadiq M. Sait** and M. Al-Darwish. 'Efficient Routing of a Class of Permutations in VLSI'. **BROWN/MIT** *Conference on Advanced Research in VLSI and Parallel Systems,* Providence, March 25-27, 1992.

19. **Sadiq M. Sait**, H. Youssef, F. Soleja, and M. S. T. Benten. 'Automated VHDL composition from AHPL'. *Fifth International Conference on Microelectronics*, **ICM'93**, December 1993, pp 220–224.

20. **Sadiq M. Sait**, M. S. T. Benten, and A. M. T Khan. 'ASIC Design from UAHPL Models'. *Fifth International Conference on Microelectronics*, **ICM'93**, December 1993, pp 237–241.

21. K. Elleithy, **Sadiq M. Sait** and M. Hasan. 'Formal Design of VLSI Systems'. *Fifth International Conference on Microelectronics*, **ICM'93**, December 1993, pp 214–219.

22. **Sadiq M. Sait**, M. S. T. Benten, and Asjad M. T. K. 'ASIC Design with AHPL'. *IEEE* **Melecon'94**, April 1994, pp 1234–1237.

23. **Sadiq M. Sait**, K. Elleithy, and M. Hasan. 'Design of a Cell Library for Formal High-level Synthesis', *IEEE* **Melecon'94**, April 1994, pp 1238–1241.

24. S. Ali, **Sadiq M. Sait**, and M. S. T. Benten. 'GSA: Scheduling and Allocation using Genetic Algorithm'. *European Design Automation Conference with Euro-VHDL*, **Euro-DAC'94**, Grenoble, September1994, pp 84-89.

25. S. Ali, **Sadiq M. Sait**, and M. S. T. Benten. 'Application of Tabu Search in High-level Synthesis of Digital Systems'. *International Conference on Electronics, Circuits and Systems,* **ICECS'94**, Cairo, December 1994, pp 423-428.

26. **Sadiq M. Sait**, A. S. Al-Mulhem, H. Youssef, and M. S. T. Benten. 'Hardware Specific Optimization in High-level Synthesis'. *International Conference on Electronics, Circuits and Systems*, **ICECS'94**, Cairo, December 1994. pp 418–422.

27. H. F. Al-Sukhni, H. Youssef, **Sadiq M. Sait**, and M. S. T. Benten. 'A New Loop Based Scheduling algorithm'. *IEEE Phoenix Conference on Computers and Communications*, **IPCCC**, March 1995, pp 76-81.

28. H. Youssef, **Sadiq M. Sait**, K. Nassar, and M. S. T. Benten. 'Performance Driven Standard-cell Placement Using the Genetic Algorithm'. *Fifth Great Lakes Symposium on VLSI*, **GLSVLSI'95**, Buffalo, USA, March 1995, pp 124-127.

29. **Sadiq M. Sait**, H. Youssef, K. Nassar, and M. S. T. Benten. 'Timing Driven Genetic Algorithm for Placement'. *IEEE Phoenix Conference on Computers and Communications*, **IPCCC**, March 1995, pp 403-409.

30. **Sadiq M. Sait**, A. A. Farooqui, G. F. Beckhoff. 'A Novel Technique for Fast Multiplication'. *IEEE Phoenix Conference on Computers and Communications*, **IPCCC**, March 1995, pp 109-114.

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32. **Sadiq M. Sait**, H. Youssef, S. Tanvir and M. S. T. Benten. 'Timing Influenced General-Cell Genetic Floorplanner'. *Asia and South-Pacific Design Automation Conference,* **ASP-DAC'95**, Japan, September 1995.

33. G. F. Beckhoff, **Sadiq M. Sait**, and A. A. Farooqui. 'Highly reconfigurable RISC data flow array processor for DSP applications'. *The 6th International Conference of Signal Processing Applications & Technology*, **ICSPAT'95**, Boston, October 1995.

34. **Sadiq M. Sait**. 'Synthesis of digital systems in VLSI', (Invited Paper and Keynote Address). *The 7th International Conference of Microelectronics*, **ICM'95**, Kuala Lumpur, December 1995.

35. A. A. Farooqui, **Sadiq M. Sait**, and G. F. Beckhoff. 'Data Flow RISC Processor'. *The 2nd Australasian Conference on Parallel and Real-Time Systems,* **PART'95**, Australia, September 1995.

36. E. Shragowitz, H. Youssef, **Sadiq M. Sait**, and H. Adiche. 'Fuzzy Genetic Algorithm for Floorplan Design'. (Invited Paper, abstract submitted to) *International Conference on Applications of Soft Computing*, **SPIE'97**, 1997.

37. **Sadiq M. Sait** H. Youssefand Munir M. Zahra. 'Tabu Search Based Circuit Optimization'. (Accepted by) *Great Lakes Symposium on VLSI*, **GLSVLSI'98**, SW Louisiana, February 1998, pp 338-343.

38. Ta-Cheng, **Sadiq M. Sait** and W. R. Cyre. 'Performance and Interface Buffer Size Driven Behavioral Partitioning for Embedded Systems'. *9th International Workshop on Rapid Systems Prototyping*, **IEEE Computer Society Sponsored**, Leuven, Belgium, April 1998.

39. Ta-Cheng Lin, Sadiq M. Sait and W. R. Cyre. 'Buffer Size Driven Partitioning for HW/SW Co-Design'. IEEE International Conference on Computer Design, ICCD'98, Austin, USA, 1998.

40. Sadiq M. Sait, Habib Youssef and Ali Hussain. Fuzzy Simulated Evolution Algorithm for Multiobjective Optimization of VLSI Placement", IEEE Congress on Evolutionary Computation", July 1999, Washington DC, pp 91-97.

41. Hasan Cam, Mostafa Abd-El-Barr, and Sadiq M. Sait. 'A High-Performance Hardware-Efficient Memory Allocation Technique and Design'. IEEE International Conference on Computer Design, ICCD'99, Austin, USA, 1999, pp 274-276.

42. H. Youssef, **Sadiq M. Sait**, and Salman Khan. "Fuzzy Simulated Evolution Algorithm for Topology Design on Campus Networks", IEEE Congress on Evolutionary Computation", July 2000, San Diego, USA,

43. Hassan Barada, **Sadiq M. Sait**, and Naved Baig. "Task Matching and Scheduling in Heterogeneous Computing Environments using Iterative Heuristics", 13th International Conference on Parallel and Distributed Computing Systems, August 2000, Las Vegas, USA.

44. **Sadiq M. Sait**, H. Youssef, H. Barada, and Ahmed Al-Yamani. "A Parallel Tabu Search Algorithm for VLSI Standard-Cell Placement", IEEE International Symposium on Circuits and Systems", May 2000, Geneva,

45. H. Barada, **Sadiq M. Sait** and N. Baig. "Task Matching and Scheduling in Heterogeneous Systems Using Simulated Evolution", 10th Heterogeneous Computing Workshop in conjunction with IPDPS 2001, San Francisco, April 2001.

46. H. Youssef, **Sadiq M. Sait**, and Salman Khan. "Fuzzy Evolutionary Hybrid Metaheuristics for Network Topology Design", International Conference on Evolutionary Multi-Criterion Optimization, EMO'01, March 7-9, 2001, ETH Zurich, Switzerland (A Springer Publication). (Accepted).

47. Habib Youssef, **Sadiq M. Sait** and Ali Hussain. Adaptive Bias Simulated Evolution Algorithm for Placement", IEEE *2001 International Symposium on Circuits and Systems*, May 2001, Sydney, Australia, pages 355-358.

48. Junaid Khan, **Sadiq M. Sait**, and Salman Khan. A Fast Constructive Algorithm For Fixed Channel Assignment Problem", IEEE *2001 International Symposium on Circuits and Systems*, May 2001, Sydney, Australia, pages 65-68.

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50. **Sadiq M. Sait**, Habib Youssef, and Junaid A. Khan. Fuzzy Evolutionary Algorithm for VLSI Placement, (Spector, L., E. Goodman, A. Wu, W.B. Langdon, H.-M. Voigt, M. Gen, S. Sen, M. Dorigo, S. Pezeshk, M. Garzon, and E. Burke, editors). 2001. Proceedings of the Genetic and Evolutionary Computation Conference, GECCO-2001. San Francisco, CA: Morgan Kaufmann Publishers. pages 1056-1063.

51. Junaid A. Khan, **Sadiq M. Sait**, and Abdulaziz S. Al-Mulhem. Algorithms for Channel Assignment Problem in Wireless Networks, SCI 2001, July 22-25, 2001, Orlando, Florida USA.

52. H. Youssef, **Sadiq M. Sait** and Salman Khan. An Evolutionary Algorithm for Network Topology Design. International Joint INNS-IEEE Conference on Neural Networks Washington DC, July 14-19, 2001.

53. Aiman Al-Maleh, **Sadiq M. Sait** and S. Z. Shazli. Evolutionary meta-heuristic for state justification in sequential ATPG. International Joint INNS-IEEE Conference on Neural Networks Washington DC, July 14-19, 2001.

54. **Sadiq M. Sait**, H. Youssef and Junaid Khan. Fuzzy Simulated Evolution for Power and Performance Optimization of VLSI Placement. International Joint INNS-IEEE Conference on Neural Networks Washington DC, July 14-19, 2001.

55. **Sadiq M. Sait**, H. Youssef Aiman El-Maleh and M. Minhas. Iterative Heuristics for Multiobjective VLSI Cell Placement. International Joint INNS-IEEE Conference on Neural Networks Washington DC, July 14-19, 2001.

56. H. Youssef, A. Almulhem, **Sadiq M. Sait**, and M. Atif Tahir. QoS-Driven Multicast Tree Generation Using Tabu Search. Proceedings of the 2001 International Symposium on Performance Evaluation of Computer and Telecommunication Systems (SPECTS 2001). Florida, July 2001.

57. **Sadiq M. Sait**, H. Youssef and Junaid Khan. Fuzzified Iterative Algorithms for Performance Driven Low Power VLSI Placement IEEE International Conference on Computer Design, ICCD'2001, Austin, September 23-26, 2001.

58. Ahmad Al-Yamani, Sadiq M. Sait, and Hassan R. Barada. "HPTS: Heterogeneous Parallel Tabu Search for VLSI Placement", IEEE Congress on Evolutionary Computation", May 2002, Honolulu, Hawaii, USA (Accepted).

59. Sadiq M. Sait, Mahmood R. Minhas, and Junaid A. Khan. "Performance and Low Power Driven VLSI Standard Cell Placement using Tabu Search", IEEE Congress on Evolutionary Computation", May 2002, Honolulu, Hawaii, USA (Accepted).

60. Junaid A. Khand and Sadiq M. Sait. "Fuzzy Aggregating Functions for Multiobjective VLSI Placement", IEEE International Conference on Fuzzy Systems", May 2002, Honolulu, Hawaii, USA (Accepted).

61. Junaid A. Khan, Sadiq M. Sait and Mahmood R. Minhas. "Fuzzy Biasless Simulated Evolution for Multiobjective VLSI Placement", IEEE Congress on Evolutionary Computation", May 2002, Honolulu, Hawaii, USA (Accepted).

Publications in Regional/National Refereed Conferences

1. **Sadiq M. Sait** and M. Masud. 'An Approach to Automate VLSI Design'. 10^{th} **NCC**, *National Computer Conference and Exhibition,* King Abdul Aziz University, Jeddah, February 1988, pp 190-205.

2. **Sadiq M. Sait** and M. Masud. 'Development of VLSI Design Facility at KFUPM'. 11^{th} **NCC** *National Computer Conference and Exhibition,* King Fahd University of Petroleum and Minerals, Dhahran, March 1989, pp 613–623.

3. M. Masud, J. Yazdani, and **Sadiq M. Sait**. 'PCB Layouts from RTL Descriptions: An Automated Approach'. 11^{th} **NCC** *National Computer Conference and Exhibition,* King Fahd University of Petroleum and Minerals, Dhahran, March 1989, pp 2–13.

4. F. A. Al-Khulaiwi and **Sadiq M. Sait**. 'Automatic Weinberger Synthesis from a UAHPL Description'. **GESS'90**, Gulf Expert Systems Symposium, Kuwait, May 1990, pp C70–C82.

5. M. A. Al-Rashed and **Sadiq M. Sait**. 'An Efficient Algorithm for Weinberger Array Folding'. **GESS'90**, Gulf Expert Systems Symposium, Kuwait, May 1990, pp C43–C57.

6. **Sadiq M. Sait**. 'From CLUs in UAHPL To Optimal Weinberger Arrays'. 12^{th} **NCC**, *National Computer Conference and Exhibition,* Riyadh, October 1990, 807–821.

7. **Sadiq M. Sait**, M. S. T. Benten, and H. Youssef. 'Modeling in VHDL for UAHPL Natives'. 13^{th} **NCC**, *National Computer Conference and Exhibition,* Riyadh, November 1992, pp 672-692.

8. **Sadiq M. Sait**, M. S. T. Benten, and A. M. T. Khan. 'VLSI CAD: The Saudi Arabian Experience'. 13^{th} **NCC**, *National Computer Conference and Exhibition,* Riyadh, November 1992, pp 611-623.

9. M. S. T. Benten, **Sadiq M. Sait**, A. Maasrani, and H. Youssef. 'RTL Structural Synthesis from Behavioral Descriptions in a Unix Environment'. 13^{th} **NCC**, *National Computer Conference and Exhibition,* Riyadh, November 1992, pp 279-299.

10. **Sadiq M. Sait**, K. Abdul Aziz and M. S. T. Benten. 'A Framework for the VLSI Implementation of a Systolic Tree Based Data Structures'. HCST, Applied Science University, Jordan, August 1994.

11. M. S. T. Benten, **Sadiq M. Sait**, A. M. T. Khan. *Load Balancing: A genetic approach*, Parallel and Distributed Computing, Kuwait, March 1995.

12. A. A. Farooqui, G. F. Beckhoff, and **Sadiq M. Sait**. 'Design, Modeling, and Implementation of a RISC Data Flow Array Processor'. Parallel and Distributed Computing, Kuwait, March 1995.

13. **Sadiq M. Sait** and Talal Maghrabi. 'Component Selection and Pipelining using Stochastic Evolution Algorithm'. 15^{th} **NCC** *National Computer Conference and Exhibition,* King Fahd University of Petroleum and Minerals, Dhahran, October 1997.

14. H. Youssef, **Sadiq M. Sait** and Osama Al-Haj Isa. 'Computer Aided Design of Structured Backbones'. 15^{th} **NCC** *National Computer Conference and Exhibition,* King Fahd University of Petroleum and Minerals, Dhahran, October 1997.

15. H. Youssef, S. M. Sait, and Salman Khan. "A Simulated Annealing Algorithm for Switched Campus Network Design", accepted for presentation at *18th National Computer Conference, NCC'2000, Dhahran, KSA*. November 2000.
16. H. Youssef, S. M. Sait, and Salman Khan. "Topology Design of Structured Campus Networks", in proceedings of the *7th IEEE Annual Technical Exchange meeting*, Dhahran, 18-19 April, 2000.
17. H. Youssef, Sadiq M. Sait, and M. Ahsan Siddiqui. "Data Flow Graph Allocation to Array Processors using Genetic Algorithm", accepted for presentation at *18th National Computer Conference, NCC'2000, Dhahran, KSA*. November 2000.
18. Salman A. Khan, Syed Z. Shazli, Junaid A. Khan, Sadiq M. Sait, " Distance Education and its Prospects in Saudi Arabia", In Proceddings of First Saudi Technical Conference and Exhibition, 18-22 Nov. 2000, Riyadh, Saudi Arabia, Vol. 1, pp 81-85.

Summary: Authored 79 conference papers, of these 61 in refereed IEEE/International conferences, and 18 in Regional/National Refereed Conferences.

Attendance and Presentations in Conferences

1. **Sadiq M. Sait**. 'A General Cell Placement Procedure for UAHPL Based DA System'. *IEEE Proceedings of* **CompEuro'87,** Hamburg, Germany, May 1987.
2. **Sadiq M. Sait** and M. Masud. 'CAD of Custom VLSI Layouts from RTL Specifications'. *30th Midwest Symposium on Circuits and Systems,* Syracuse, USA, August 1987.
3. **Sadiq M. Sait**, M. Masud, and G. F. Beckhoff. 'Heuristics for Automatic Routing of Cells Placed by UAHPL Silicon Compiler'. *Second International Conference on Microelectronics and Microcomputers,* Menouf, Egypt, December 1987.
4. M. A. Kulaib, G. F. Beckhoff, and **Sadiq M. Sait**. 'CMOS Programmable Length First-In, First-Out Memory'. *Second International Conference on Micro-Electronics and Micro-computers,* Menouf, Egypt, December 1987.
5. **Sadiq M. Sait** and M. Masud. 'An Approach to Automate VLSI Design'. 10^{th} **NCC**, *National Computer Conference and Exhibition,* King Abdul Aziz University, Jeddah, February 1988.
6. **Sadiq M. Sait** and M. Masud. 'Development of VLSI Design Facility at KFUPM. 11^{th} **NCC** *National Computer Conference and Exhibition,* King Fahd University of Petroleum and Minerals, Dhahran, March 1989.

7. F. A. Al-Khulaiwi and **Sadiq M. Sait**. 'Automatic Weinberger Synthesis from a UAHPL Description'. **GESS'90**, Gulf Expert Systems Symposium, Kuwait, May 1990.

8. M. A. Al-Rashed and **Sadiq M. Sait**. 'An Efficient Algorithm for Weinberger Array Folding'. **GESS'90**, Gulf Expert Systems Symposium, Kuwait, May 1990.

9. **Sadiq M. Sait**. 'From CLUs in UAHPL To Optimal Weinberger Arrays'. 12^{th} **NCC**, *National Computer Conference and Exhibition,* Riyadh, October 1990, 807–821.

10. **Sadiq M. Sait**, M. S. T. Benten, and A. M. T. Khan. 'VLSI CAD: The Saudi Arabian Experience'. 13^{th} **NCC**, *National Computer Conference and Exhibition,* Riyadh, November 1992.

11. **Sadiq M. Sait**, H. Youssef, F. Soleja, and M. S. T. Benten. 'Automated VHDL composition from AHPL'. *Fifth International Conference on Microelectronics*, **ICM'93**, Dhahran, December 1993.

12. **Sadiq M. Sait**, M. S. T. Benten, and A. M. T Khan. 'ASIC Design from UAHPL Models'. *Fifth International Conference on Microelectronics*, **ICM'93**, Dhahran, December 1993.

13. K. Elleithy, **Sadiq M. Sait** and M. Hasan. 'Formal Design of VLSI systems'. *Fifth International Conference on Microelectronics*, **ICM'93**, Dhahran, December 1993.

14. S. Ali, **Sadiq M. Sait**, and M. S. T. Benten. 'GSA: Scheduling and Allocation using Genetic Algorithm'. *European Design Automation Conference with Euro-VHDL*, **Euro-DAC'94**, Grenoble, France, September1994.

15. H. F. Al-Sukhni, H. Youssef, **Sadiq M. Sait**, and M. S. T. Benten. 'A New Loop Based Scheduling algorithm'. *IEEE Phoenix conference on Computers and Communications*, **IPCCC**, Arizona, USA, March 1995.

16. **Sadiq M. Sait**, H. Youssef, K. Nassar, and M. S. T. Benten. 'TDGAP: Timing Driven Genetic Algorithm for Placement'. *IEEE Phoenix conference on Computers and Communications*, **IPCCC**, Arizona, USA, March 1995.

17. **Sadiq M. Sait**, A. A. Farooqui, G. F. Beckhoff. 'A Novel Technique for Fast Multiplication'. *IEEE Phoenix conference on Computers and Communications*, **IPCCC**, Arizona, USA, March 1995.

18. H. Youssef, **Sadiq M. Sait**, and K. Al-Farrah. 'Timing Influenced Force Directed Floorplanning'. *European Design Automation Conference with Euro-VHDL*, **Euro-DAC'95**, Brighton, England, September 1995.

19. **Sadiq M. Sait**. 'Synthesis of digital systems in VLSI', (Invited Paper and Keynote Address). *The 7th International Conference of Microelectronics*, **ICM'95**, Kuala Lumpur, Malaysia, December 1995.

20. M. S. T. Benten, **Sadiq M. Sait**, A. M. T. Khan. *Load Balancing: A genetic approach*, Parallel and Distributed Computing, Kuwait, March 1995.

21. Sadiq M. Sait, Habib Youssef and Ali Hussain. Fuzzy Simulated Evolution Algorithm for Multiobjective Optimization of VLSI Placement", IEEE Congress on Evolutionary Computation", July 1999, Washington DC.

22. Hasan Cam, Mostafa Abd-El-Barr, and Sadiq M. Sait. 'A High-Performance Hardware-Efficient Memory Allocation Technique and Design'. IEEE International Conference on Computer Design, ICCD'99, Austin, USA, 1999, pp 274-276.

23. **Sadiq M. Sait**, H. Youssef, H. Barada, and Ahmed Al-Yamani. "A Parallel Tabu Search Algorithm for VLSI Standard-Cell Placement", IEEE International Symposium on Circuits and Systems", May 2000, Geneva,

24. Habib Youssef, **Sadiq M. Sait** and Ali Hussain. Adaptive Bias Simulated Evolution Algorithm for Placement", IEEE *2001 International Symposium on Circuits and Systems*, May 2001, Sydney, Australia.

25. Junaid Khan, **Sadiq M. Sait**, and Salman Khan. A Fast Constructive Algorithm For Fixed Channel Assignment Problem", IEEE *2001 International Symposium on Circuits and Systems*, May 2001, Sydney, Australia.

26. Aiman H. El-Maleh, **Sadiq M. Sait**, and Syed Z. Shazli. Test Pattern Generation. Proceedings of the Genetic and Evolutionary Computation Conference, GECCO-2001. San Francisco, CA: Morgan Kaufmann Publishers.

27. **Sadiq M. Sait**, Habib Youssef, and Junaid A. Khan. Fuzzy Evolutionary Algorithm for VLSI Placement, Proceedings of the Genetic and Evolutionary Computation Conference, GECCO-2001. San Francisco, CA: Morgan Kaufmann Publishers.

Summary: Of the 79 conference papers we authored/co-authored, I presented 27 of these in International/National meetings.

Lectures, Seminars, & Invited Talks

1. Invited talk in Fredrich Alexander University, W.Germany, entitled 'VLSI Mask Generation from Register Transfer Level Descriptions' May 1987.

2. Invited talk in IBM Research Laboratory: Rushlikon, Zurich, Switzerland entitled 'UAHPL Based VLSI Design Automation', May 1987.

3. Invited talk in the *Second International Conference on Micro-Electronics*, Menoufia University, Menouf, Egypt, entitled 'Teaching Methods and Experience', December 1987.

4. Seminar in the College of Computer Science and Engineering, KFUPM, entitled 'Introduction to VLSI System Design', 1988.

5. Seminar in the College of Computer Science and Engineering, KFUPM, entitled 'Synthesis of Weinberger Arrays', 1989.

6. Seminar in the ACM Chapter, Dhahran, entitled 'VLSI DA at KFUPM', 1990.

7. Seminar in the College of Computer Science and Engineering, Dhahran, entitled 'Chip-Smith's Tools', 1991.

8. Seminar in the Department of Electrical Engineering entitled 'VLSI System Design', 1992.

9. Lecture in English Language Center, KFUPM, entitled 'Computer Engineering: The Discipline of Future'. March 1994 and March 1995 (repeated).

10. Seminar in *MiniSymposium on Optimization*, KFUPM, entitled 'Experience with Iterative Algorithm (On Some Optimization Problems in Computer Engineering), May 1995.

11. Invited Keynote address in *Seventh International Conference on Microelectronics*, Kuala Lumpur, Malaysia, entitled 'Synthesis of VLSI Digital Systems', December 1995.

12. Lecture during *Fourteenth Annual Computer Exhibition*, Dhahran, 'Computer Evolution', April 1996.

13. Contributed to Lecture during *Workshop on Fuzzy Logic and Its Applications*, Dhahran, entitled 'A Fuzzy Genetic Algorithm for Floorplan Design', December 1996 (presentation made by Dr. H. Youssef).

14. Seminar on "Research Grants at KFUPM" November 1999, KFUPM, Dhahran.

15. Seminar on "Iterative Heuristics for Timing and Low Power VLSI Standard Cell Placement", November 2000, KFUPM, Dhahran.

Sample Citations

Citations in Journal/Conferences/Technical Reports

1. M. M. Abdallah, and A. I. Alabdulaaly. 'The Role of Research in The Advancement of Computer Technology in Saudi Arabia'. *Proceedings of* 13^{th} *NCC, Riyadh*, Vol-I, pp 73-89. (See pg 82 and pg 89), 1992, {Cited work: Item -11}.

2. Alnuweiri H. M. 'A New Class of Optimal Bounded-Degree VLSI Sorting Networks'. *IEEE Transactions on Computers*, Vol 42, No. 6, pp 746-752, 1993, {Cited work: Item -18}.

3. A. Amin and H. Youssef. 'Design and Development of a new Family of Nonvolatile SRAM-Based FPGAs'. Progress Report No. 1 of KACST Project AR-14-67, October 1994. -3}.

4. Alnuweiri H. M. 'Optimal VLSI Networks for Multidimensional Transforms'. *IEEE Transactions on Parallel and Distributed Systems*, Vol 5, No. 7, pp 763-769, 1994, {Cited work: Item -18}.

5. A. Amin and H. Youssef. 'Design and Development of a new Family of Nonvolatile SRAM-Based FPGAs'. Progress Report No. 2 of KACST Project AR-14-67, March 1995. {Cited work: Item -3, -29}.

6. A. Amin and H. Youssef. 'Design and Development of a new Family of Nonvolatile SRAM-Based FPGAs'. Progress Report No. 3 of KACST Project AR-14-67, November 1995. {Cited work: Item -3, -31}.

7. K. Elleithy and A. Amin. 'A Formal Methodology for Parallel VLSI Algorithm Design'. Final Progress Report, KACST Project AR-13-11, October 1995. {Cited work: Item -3}.

8. Jose Augusto Limo. 'A Cell Orientation Based Placement and Routability Evaluation Model'. *International Conference on Microelectronics*, pp 273-277, December 1996. {Cited work: Item -3}.

9. Alda Reis Lopes, Jose Augusto Limo, P. R. Henriques. 'Using Syntactic Methods in Global Routing Problem Formulation'. *International Conference on Microelectronics*, pp 279-283, Cairo, December 1996. {Cited work: Item -3}.

10. A. Amin and H. Youssef. 'Design and Development of a new Family of Nonvolatile SRAM-Based FPGAs'. Progress Report No. 4 of KACST Project AR-14-67, November 1996. {Cited work: Item -2, -3, -29}.

11. A. S. Al-Mulhem, A. Amin and H. Youssef. 'SELF-MAP: Stochastic Evolution LUT-FPGA Technology Mapper'. (Pre-Print of Journal/Conference publication provided by the authors, submitted to *IEEE Transactions on VLSI, and ICCAD*), January 1997. {Cited work: Items -2}.

12. Zhang, C. X and Mlynski, D. A. *Mapping and Hierarchical Self-Organizing Neural Networks for VLSI Placement.* IEEE Transactions on Neural Networks, Vol. 8, Issue 2, pp 299-314, 1997. {Cited work: Item -3}.

13. Jiangzhong Shi, Akash Randhar, and Dinesh Bhatia. 'Macro Block Based FPGA Floorplanning. *The Proceedings of 10thIEEE International Conference on VLSI Design*, January 1997, pp 21-26. {Cited work: Items -3, and -31}.

14. M. J. S. Smith. 'Application-Specific Integrated Circuits'. *Addison-Wesley Longman Inc*, January 1997 (Text Book). {Cited work: Items -3}.

15. N. Togawa, et.al. 'An Incremental Placement and Global Routing Algorithm for Field-Programmable Gate Arrays. 1998 IEEE International ASP'DAC'98 pp 519-526. {Cited work: Item -3}.

16. M. Ohmura. 'An Initial Placement Algorithm for 3-D VLSI. *1998 ISCAS, International Symposium on Circuits and Systems*, May 1998, Monetery, California. {Cited work: Item -3}.

17. R. Sedaghat-Maman. 'Fault Emulation with Optimized Assignment of Circuit Nodes to Fault Injectors. *1998 ISCAS, International Symposium on Circuits and Systems*, May 1998, Monetery, California. {Cited work: Item -3}.

18. Jiangzhong Shi and Dinesh Bhatia. 'Performance Driven Floorplanning for FPGA Based Designs. *1997 ACM Fifth International Symposium on Field-Programmable Gate Arrays*, February 1997, Monetery, California, pp 112-118. {Cited work: Item -31}.

19. Claudia I. Horta and Jose A. Lima. *Slicing and Non-Slicing, Unified and Rotation Independent, Algebraic Representation of Floorplans.* 1997 IEEE Euromicro 97: New Frontiers of Information Technology, pp 265-272. {Cited work: Item -3}.

20. H. Murata et al. *A Mapping from Sequence -Pair to Rectangular Dissection.* 1997 IEEE International ASP'DAC'97 pp 625-633. {Cited work: Item -3}.

21. S. Wakabayashi and T. Koide. *Timing-Driven Pin Assignment with Improvement of Cell Placement in Standard Cell Layout.* 1997 IEEE International Symposium on Circuits and Systems. pp 1552-1555. {Cited work: Item -3}.

22. Y. S. Kim and K. S. Yoon. *An Analog Layout Floorplanner Using Its Parameterized Module Layout Structure.* 1996 Proceedings of IEEE Asia Pacific Conference on Circuits and Systems. pp 397-400. {Cited work: Item -3}.

23. S. Wakabayashi, Y. Kishimito and T. Koide. *An Optimal Pin Assignment Algorithm with Improvement of Cell Placement in Standard Cell Layout.* 1996 Proceedings of IEEE Asia Pacific Conference on Circuits and Systems. pp 381-384. {Cited work: Item -3}.

24. R. Moreno, R. Hermida, M. Fernandez, and H. Mecha. 'A unified approach for scheduling and allocation'. *Integration, The VLSI Journal*), Vol 23, October 1997, pp 1-35. {Cited work: Items -24}.

25. M. Mir and M. Hasan Imam. 'A Heuristic-cum-Analytic Technique for Building Block Layout Optimization'. *Umm Al-Qura University Journal*), 1998. {Cited work: Items -3}.

26. M. Benmohammed, P. Kission, M. Rahmouni and A.A Jerraya. 'Programmable Architecture Generation in High-Level Synthesis Environment'. Submitted to *Arabian Journal for Science and Engineering*, 1996, {Cited work: Item -15}.

27. Dinesh Bhatia. 'Hierarchical Floorplanning and Placement for FPGAs. (Submitted to *The IEEE International Conference on Computer Aided Design* (ICCAD), manuscript down-loaded from authors Home-Page on the Internet), November 1996, {Cited work: Items -3, and -31}.

28. Theodre Manikas and James T. Cain. 'Genetic Algorithms vs. Simulated Annealing: A Comparison of Approaches for Solving the Circuit Partitioning Problem. Technical Report 96-101, University of Pittsburgh, May 1996, {Cited work: Item -29}.

29. M. Benmohammed, P. Kission, C. Liem and A.A Jerraya. 'Generating Reprogrammable Microcoded Controllers within a High-Level Synthesis Environment'. Submitted to *Arabian Journal for Science and Engineering*, 1996, {Cited work: Item -15}.

30. K. Ohmori, P.W. Eklund and J. Daalder. 'Simultaneous Scheduling and Allocation in High-Level Synthesis Using A Genetic Algorithm'. *IEEE International Conference on Computer Aided Design*, Linz, Austria, September 1996. {Cited work: -24}.

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40. M. Moizuddin. 'Solution of the Resource Constrained Activity Networks' MS Thesis, Systems Engineering Department. October 1996, {Cited works: Items -2 and -3}.

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1. **Sadiq M. Sait**. 'An Integrated Design Automation System for Generating VLSI Layouts'. KACST Project Report Number 1, December 1991.
2. M. S. T. Benten and **Sadiq M. Sait**. 'PTT Classified Research Project'. Submitted to The Office of The Rector.
3. **Sadiq M. Sait** and M. S. T. Benten. 'An Integrated Design Automation System for Generating VLSI Layouts'. KACST Project Report Number 2, June 1992.
4. **Sadiq M. Sait** and M. S. T. Benten. 'An Integrated Design Automation System for Generating VLSI Layouts'. KACST Project Report Number 3, Dec 1992.
5. M. S. T. Benten, **Sadiq M. Sait**, and H. Youssef. 'Design and Implementation of an Integrated Design Automation Environment for High-level Silicon Compilation'. KFUPM Research Committee Project Report Number 1, 1992.
6. **Sadiq M. Sait** and M. S. T. Benten. 'An Integrated Design Automation System for Generating VLSI Layouts'. KACST Project Report Number 4, June 1993.
7. **Sadiq M. Sait** and M. S. T. Benten. 'An Integrated Design Automation System for Generating VLSI Layouts'. KACST Project Report Number 5, Dec 1993.
8. M. S. T. Benten, **Sadiq M. Sait**, and H. Youssef. 'Design and Implementation of an Integrated Design Automation Environment for High-level Silicon Compilation'. KFUPM Research Committee Project Report Number 2, 1993.
9. M. S. T. Benten, **Sadiq M. Sait**, and H. Youssef. 'Design and Implementation of an Integrated Design Automation Environment for High-level Silicon Compilation'. KFUPM Research Committee Project Report Number 3, 1994.
10. H. Youssef, **Sadiq M. Sait**, and M. S. T. Benten. 'Analysis and Physical Design Tools for Solving Timing Problems in VLSI Design'. KFUPM Project Report 1, October 1994.
11. **Sadiq M. Sait** and M. S. T. Benten. 'An Integrated Design Automation System for Generating VLSI Layouts'. KACST Final Project Report, Dec 1994.
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Master of Sciences Thesis Supervision

1. Jaweed Yazdani. A Software Tool To Generate PCB Layout from RTL Specifications using SSI/MSI Components. Spring 1987, **Member**, (ICS Department).

2. Ali F. Damati. A Systolic Algorithm for VLSI Design of a Viterbi Decoder. Spring 1988, **Member**, (EE Department).

3. Abdul Aziz Hamed. Data Protection in a Distributed Computer Environment. 1990, **Member**, (ICS Department).

4. Asjad M.T. Khan. VLSI Implementation of Petri-nets Models for a Class of Digital Systems. Spring 1991, **Co-Chairman**, (EE Department).

5. A. Al-Maasrani. Priority-Based Scheduling and Evaluation of Precedence Graphs with Communication Times. August 1993, **Member**.

6. Masud-ul Hasan. Back-End Design of a Formal High-Level Synthesis System. June 1993, **Chairman**.

7. H. Sukhni. C-Based High Level Synthesis. Fall 1993 **Co-Chairman**.

8. A. Al-Mulhem. Hardware Specific Optimization on RTL Descriptions. Fall 1993. **Chairman**.

9. K. Nassar. Timing Driven Genetic Algorithm for Standard-Cell Placement. June 1994, **Chairman**.

10. M. A. Khalid. A Framework for the VLSI Implementation of Systolic Tree Data Structures. Sept. 1994, **Chairman**.

11. E. Hubbi. Intermediate Forms in High Level Synthesis Nov. 1994. **Chairman**.

12. K. Al-Farrah. Timing Influenced Force Directed Floorplanning. Fall 1994, **Co-Chairman**.

13. S. T. Khan. Timing Driven Genetic Algorithm for Floorplanning. Fall 1994, **Chairman**.

14. H. Abu-Saleh. A General Cell VLSI Design System. Fall 1994, **Chairman**.
15. Shahid Ali. Scheduling and Allocation in High-level Synthesis Using Genetic Algorithm. Spring 1994, **Co-Chairman**, (ICS Department).
16. Asaf Maruf. Design and Modeling of a Real-Time RISC Processor in VHDL. Spring 1994, **Member**.
17. M. A. Abdul-Hai. Subcube Reliability of Modular Fault Tolerant Hypercube Based Interconnection Networks. Spring 1995, **Member**.
18. M. Abu-Mutlaq. Dataflow Processor for Back Propagation Neural Networks. Spring 1995, **Co-Chairman**.
19. Ahmed Awad. Design and Implementation of a Simulator for Systolic Arrays. 1995, **Chairman**.
20. F. Soleja. A VHDL Composer from AHPL Descriptions. Fall 1995, **Chairman**, (ICS Department).
21. Amir A. Farooqui. Design, Modeling and VLSI Implementation of a RISC Data Flow Array Processor. Spring 1994-5, **Co-Chairman**, (EE Department).
22. Amir Hashmi. Timing Driven Global Routing for Standard Cell Design. Spring 1994-5, **Member**, (ICS Department).
23. Nayyar Hasan. On the Synthesis and Optimization of MVL Functions. Spring 1994-5, **Member**.
24. K. Abbad. Tabu Search and Stochastic Evolution: A Comparative Study. Fall 1995, **Co-Chairman**.
25. Farook M. High-level Synthesis using Stochastic Evolution Algorithm. Fall 1995, **Co-Chairman**, (ICS Department).
26. Adnan Ahmed Khan. Development of a Congestion Control Strategy for ATM Networks. Spring 1995, **Member**, (COE Department).
27. Sabih M. Al-Sayed. Traffic Control Strategy for ATM Networks. Spring 1995, **Member**, (COE Department).
28. Ammar Enaya. Interfacing Connection Legacy LANs to the Connection Oriented ATM Network-Problems and Solutions. Fall 1999, **Member**, (COE Department).
29. Mohsin Nadeem. Evolution Based Scheduling of DAGs with Communication. Fall 1996, **Member**, (COE Department).
30. Talal Al-Kharobi. Fuzzy Logic Based FPGA Routing. Spring 1997, **Member**, (COE Department).

31. Hakim Adiche. Fuzzy Genetic Floorplanning. Spring 1996, **Co-Chairman**, (COE Department).

32. Taisir Al-Marhoun. Testing and Evaluation Methodology of ATM Systems. Spring 1998, **Member**, (COE Department).

33. Osama Al-Hajj Isa. Computer Aided Topology Design of Structured Computer Network Backbones. Fall 1999, **Co-Chairman**, (COE Department).

34. Ahmed Nazih. Genetic Algorithm for Partial Scan Testing. Fall 1999, **Chairman**.

35. Munir Zahra. An Optimization of Mixed CMOS/BiCMOS Circuits Using Tabu Search. 1998, **Chairman**.

36. Ahmed Bin-Mahfoodh. Parallel Scheduling for Parallel Applications. Spring 1998, **Co-Chairman**, (ICS Department).

37. Ali Syed Hussain. VLSI Standard Cell Placement using Fuzzy Simulated Evolution Algorithm. Spring 1998, **Chairman**, (COE Department).

38. Ahmad A. Al-Yamani. A Parallel Tabu Search Algorithm for VLSI Standard Cell Placement. May 1999, **Chairman**, (COE Department).

39. Ahsan Siddiqui. Data Flow Graph allocation to Array Processors using Heuristics. Fall 1999, **Chairman**, (COE Department).

40. Mirza Naved Ali Baig. Task Matching and Scheduling in Heterogeneous Computing Environments using Iterative Heuristics. May 1999, **Co-Chairman**, (COE Department).

41. Salman Khan. Topological Design of Enterprise Networks. Fall 1999, **Co-Chairman**, (COE Department).

42. Junaid Asim Khan. Evolutionary Algorithms for Low Power VLSI Standard Cell Placement. **Co-Chairman**, (EE Department). [IP].

43. Syed Zafar Shazali. Experimenting with Evolutionary meta- heuristic for state justification in sequential ATPG. **Co-Chairman**, (COE Department). [IP].

44. Minhas Mehmood-ur-Rehman. Iterative Algorithms for Timing and Low Power Driven VLSI Standard Cell Placement. **Chairman**, (COE Department). [IP].

45. Atif Taher. QoS Driven Multicast Routing Algorithm. **Member**, (COE Department). [IP].

46. Yassir Obeid M. Quality of Service Routing. **Member**, (COE Department).

47. A. Barnawi. Mutlicast Routing Protocol with Partical Flooding for Ad-Hoc Wireless Networks. Fall 2000-2001, **Member**, (COE Department).

48. A. Ali-Suwaiyan. A Novel Test Set Relaxation Technique for Combinatorial Circuits. Spring 2001, **Member**, (COE Department) [IP].

49. Reslan Al-Abaji. Evolutionary Techniques for Multiobjective Netlist VLSI Partitioning. Spring 2001, **Chairman**, (COE Department) [IP].

50. Ahmer Zakir. Topological Optimization of Computer Networks Subject to Reliability and Fault Tolerance Constraints. Spring 2001, **Member**, (COE Department) [IP].

Funded Projects

1. **Sadiq M. Sait**, H. Youssef and Aiman El-Maleh. 'Iterative Heuristics for Timing & Low Power VLSI Standard Cell Placement'. Principal Investigator of KFUPM Research Committee sponsored. Budget: SR 150,800/-. Proposal accepted, to begin in January 2001.

2. **Sadiq M. Sait**, Khalid Al-Tawil and Mr. Shahid Ali. *Use and Effect of Internet in Saudi Arabia.* Two year Project. Proposal Accepted in November 1999. Budget: SR.486,500/-.

3. **Sadiq M. Sait** and H. Youssef. *General Iterative Algorithms for Combinatorial Optimization.* One year Book Project, KFUPM Research Committee. Project Budget: SR 167,600/- (US$ 44,700/-). (**Investigator**, Status: Proposal accepted by IEEE Computer Society Press, California. Contracts signed with publisher in May 1996. Completed in December 1999).

4. Abdallah Al-Sukairi, **Sadiq M. Sait** and N. Darwish. *Electronic Publishing of The Arabian Journal for Science and Engineering.* One year Project. Proposal Submitted in January 1997. Requested Budget: SR 226,400/- (US$ 60,375/-). (**Co-Investigator**, Status: Work completed, awaiting approval of the AJSE board).

5. H. Cam, **Sadiq M. Sait**, H. Youssef, and M. S. T. Benten. *Adaptive Data-Control Driven Reconfigurable Processor Arrays.* Three year KFUPM Project. # COE/ARRAYS/177, Budget: SR 647,200/- (US$ 172,600/-). (**Co-Investigator**, Status: In Progress, one progress report submitted in June 1996).

6. H. Youssef, **Sadiq M. Sait**, and M. S. T. Benten. *Analysis and Physical Design Tools for Solving Timing Problems in VLSI Design.* Two year KFUPM Project. # COE/VLSI DESIGN/162, Project Budget: SR 438,500/- (US$ 117,000/-). (**Co-Investigator**, Status: Final Report submitted in July 1996).

7. M. S. T. Benten, **Sadiq M. Sait**, and H. Youssef. *Design and Implementation of an Integrated Design Environment for High Level Silicon Compilation.* Three year KFUPM Project. Project # COE/DESIGN/145, Budget: SR 407,000/- (US$ 108,500/-). (**Co-Investigator**, Status: Completed in March 1995).

8. **Sadiq M. Sait** and H. Youssef. *VLSI Physical Design Automation: Theory and Practice.* One year Book Project. Project # COE/VLSI DESIGN/163, Budget: SR 149,800/- (US$ 40,000/-). (**Investigator**, Status: Completed in December 1994).

9. **Sadiq M. Sait** and M. S. T. Benten. *An Integrated VLSI Design Automation System for Generating VLSI Layouts.* Two and half year KACST Funded Research Project. Project # AR-11/21, Budget: SR 371,500/- (US$ 99,000/-). (**Investigator**, Status: Completed in December 1993, Final revised report submitted in December 1994).

10. M. S. T. Benten and **Sadiq M. Sait**. 'Detection and Monitoring of Facsimile Activities in the Saudi Telephone System'. Classified Research Project for PTT, assigned by The Rector of KFUPM, 1992-1993. (**Co-Investigator**, Status: Completed in December 1993).