COE 202, Fall 2016

Verilog Assignment 2

Due: Thursday, January 5, at 11 am (during class time)

Q1. Modeling a simple ALU

It is required to design an ALU circuit that receives two 16-bit input numbers **A[15:0]** and **B[15:0]**, and produces a 16-bit output **Z[15:0]** and a carry output **Cout**. The circuit implements the following functions based on the values of the 3-bit selection input **S[2:0]**:

Select Input S[2:0]	Function
0 0 0	Z = A + B
0 0 1	Z = A – B
0 1 0	Z = A + B + 1
0 1 1	Z = A – B – 1
1 0 0	Z = A & B
1 0 1	Z = A | B
1 1 0	Z = A ^ B
1 1 1	Z = ~(A | B)

For the last four logic functions, the output **Cout** should be zero.

a) [4 marks] Show the block diagram design of your circuit using components like Adder, Multiplexor, etc. as needed. Use only one adder in your solution.
b) [5 marks] Model the Adder and the Multiplexor modules in Verilog separately using continuous assignment statements.
c) [5 marks] Model the ALU by instantiating components according to your block diagram.
d) [6 marks] Write a Verilog test bench to test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness. For each function, test at least 2 input combinations of your choice to demonstrate correct functionality of the ALU.

Q2. Modeling a Synchronous Sequential Circuit

It is required to design a synchronous sequential circuit that receives a serial input **X** (bit stream) and produces a serial output **Z**. The output **Z** is set to **1** when the circuit detects either the sequence **1010** or the sequence **1001**. Assume that the detection of sequences is overlapping. The flip-flops should have an asynchronous reset input to reset the circuit to its initial state. The following is an example of an input/output bit stream:

Input Bit Stream **X**	**1 0 1 0 1 0 0 1 0 1 0 0 0**
Output Bit Stream **Z**	**0 0 0 1 0 1 0 1 0 0 1 0 0**

a) [5 marks] Design a **Mealy** state diagram of the sequence detector.

b) [5 marks] Derive the next state and output equations and draw a circuit diagram of the sequential circuit using minimal number of D flip flops and logic.

c) [7 marks] Write a structural Verilog model of your sequential circuit by first modeling the D Flip-Flop as a separate module. Then, instantiate the D Flip-Flops and model the next state and output equations using continuous assign statements.

d) [5 marks] Write a test bench that tests your structural Verilog model in (**c**) using the above input sequence. Verify that your circuit produces the correct output. Show snapshots of the generated waveforms in your report.

e) [5 marks] Write a behavioral Verilog model that models your state diagram in (a).

f) [3 marks] Use the test bench developed in (**d**) to test the correctness of your behavioral model developed in (**e**). Verify that your behavioral model produces the correct output. Show snapshots of the generated waveforms in your report.

This assignment can be solved either individually, or as a group of two students. Include snapshots of simulation output to illustrate the correctness of your circuit. Submit your solution as a word document along with the Verilog code.

A Soft copy of the word document and Verilog code should be submitted on Blackboard. In addition, a hard copy of the word document should be submitted in class.