COE 202, Fall 2016

Verilog Assignment 1: Modeling Boolean Functions

Due: Thursday, November 10, at 11 am (during class time)

1. Write a Verilog description of a circuit specified by the following Boolean functions:

$x = a(cd + b) + bc'$

$y = (a \oplus b)(c + d')$

$z = ((a + b)(c + d'))'$

a) Use continuous assignment statements to describe the above equations. Do not assign any delay to *x*, *y*, or *z*.

b) Use gate-level description to describe the above equations without modification. Use a NAND gate for the output *z*. Assign a delay of 1ns to a NOT gate, a delay of 2ns to AND, NAND, OR, and a delay of 3ns to XOR.

c) Write a test bench to test the two modules of parts (a) and (b). Exhaustive testing should be used. All the sixteen possible combinations of inputs *a*, *b*, *c*, and *d* should be used to produce outputs *x*, *y*, and *z*.

d) Run the simulator. Examine the waveforms to verify the correctness of outputs *x*, *y*, and *z*. Record the delays of *x*, *y*, and *z* for the gate-level description. Save different snapshots of the waveforms.

e) Submit a report (Word document) that should contain:

i. The Verilog module descriptions of parts (a) and (b)
ii. The test benches of parts (a) and (b)
iii. The timing diagrams (waveforms) taken directly as snapshots from the simulator. Have as many snapshots as needed to cover all the test cases.
iv. Discussion about the time delays of outputs *x*, *y*, and *z*.

A soft copy of the report and Verilog code should be submitted on Blackboard and a hard copy should be submitted in class.

Important Note: the Verilog code and simulation results should be your own individual work. Detected cheating cases (copying) will receive a grade of zero, including those who shared their work with others.